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Gate Array for Brushless Servodrive

Abstract: A chip set for highly dynamic servodrives has been developed. Its first application is a very compact, intelligent, CAN-controlled brushless AC servodrive. It can, however, be used for DC, brushless DC and induction servodrives as well. Main tasks of the chips are the calculation of rotor position, torque and current control as well as pulse-width modulation. The chip set not only enables the construction of economic and intelligent servodrives with high dynamics but, in addition, it considerably improves the reliability of the drives by drastic reduction of the component count.

Keywords: servodrive, ASIC, CAN, RISC, CORDIC, resolver converter, current control, reliability.

Introduction

The chip set ND30 was developed by the drive manufacturer Novotron (Ludwigsburg/Germany) and the ASIC-foundry Institute for Microelectronics Stuttgart (IMS CHIPS, Germany). The objective of the development was to upgrade the existing highly dynamic and intelligent servodrive ND21 while optimizing its volume, functionality, reliability and manufacturing costs.

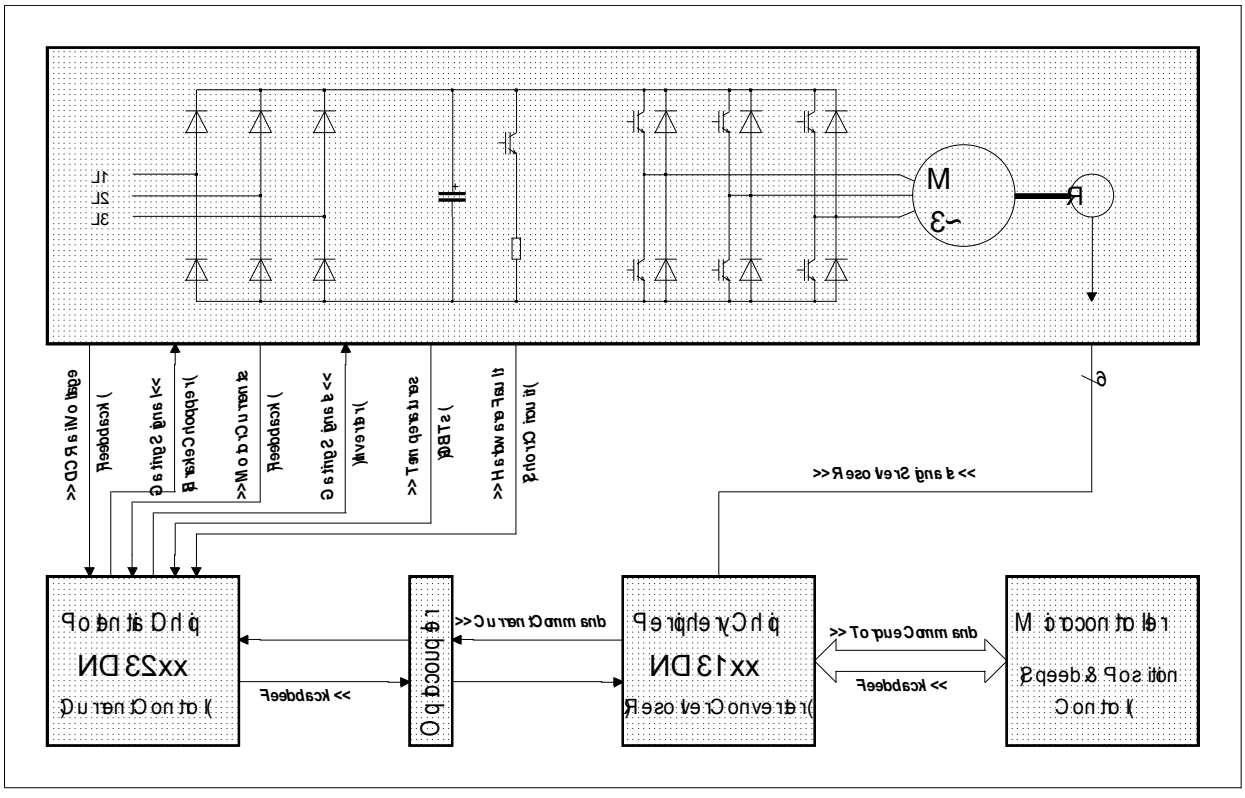

Figure 1: Drive control with the chip set ND30

In order to lower the manufacturing costs a drastic reduction of the component count was attempted. This way not only expenses for components and assembly can be saved. By highly integrated circuit design considerably smaller volume has been achieved, consequently cheaper encasement, PCB and mechanical design. When realizing brushless servodrives certain functions involve rather high expenses. Especially expensive are: The resolver converter, current measurement modules and optocouplers for galvanic isolation. The new chip set has reduced these expenses to a fraction because both resolver converter and the current measurement functions have been integrated into the chips and due to the serial data bus the isolation could be implemented using only two optocouplers.

High integration means less components and solder seams, therefore, less defect sources. To achieve better reliability and to reduce test and service expenses, numerous diagnostic features have been integrated into the chips. So the drive itself can detect and localize defects in the circuitry. Also there are fail-safe functions integrated.

In order to keep costs low while being most flexible a universal microcontroller was intentionally not integrated (Fig. 1). However, several simple but time-consuming chores which have to be performed frequently (e.g. coordinate transformations) have been realized in hardware. This extended the functionality of the drive considerably (position control, bus communication, integrated PLC, etc.) without using an expensive processor.

The chip set consists of two mixed signal ASICs. One of them is called potential chip because it is at the negative DC-rail of the power stage. The other one is the periphery chip which is located at the potential of the microcontroller, electrically isolated from the power stage of the inverters.

THE POTENTIAL CHIP

The potential chip ND32xx controls and supervises the power switches (IGBTs or MOSFETs) of the inverter and of the brake chopper (Fig. 2).

The Serial Data Bus

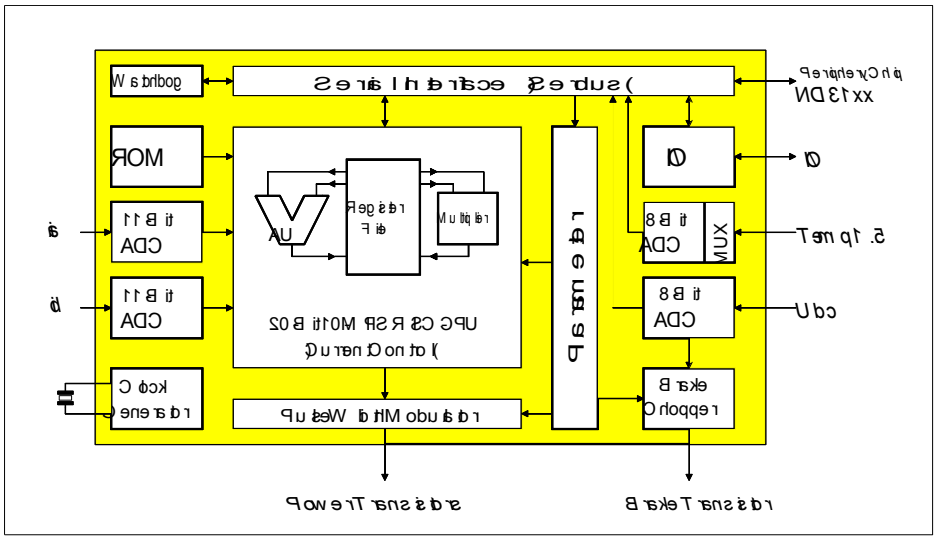

Figure 2: Potential chip ND3202

The command values for the motor currents and the limits of the bus voltage are transmitted from the periphery chip via a fault tolerant serial bus. The potential chip sends measured values of current, voltage and temperature back to the periphery chip. Also by means of this bus different functions of the chip can be parametrized on-line (Fig. 3). In order to enable galvanic isolation while maintaining high-speed data transfer, optocouplers with a transfer rate of 10 Mbit/s were chosen. Fault tolerant operation is assured by means of CRC code and acknowledgement bits.

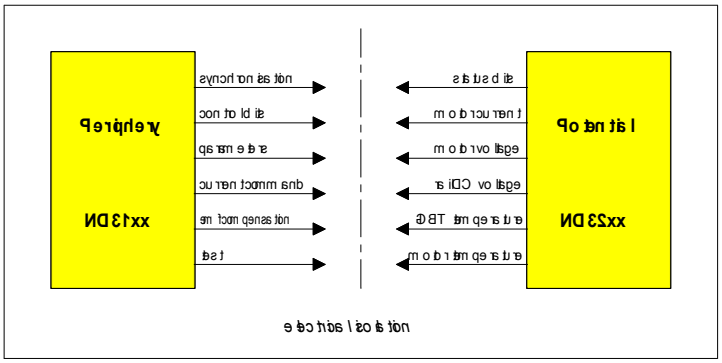

Figure 3: Data transfer between both chips

The Modulator

The 3-phase pulse-width modulator controls the six power transistors of the inverter. This modulation converts the DC bus voltage into a rotating AC voltage with variable frequency and amplitude. The resolution of the modulator is 9 bit. Its switching frequency, minimum switch-on time, dead-time between switching on and off in a branch are programmable. With symmetrical limitation of the voltage command values (Fig. 4) as well as with star voltage shifting an optimum control of the modulator is attained.

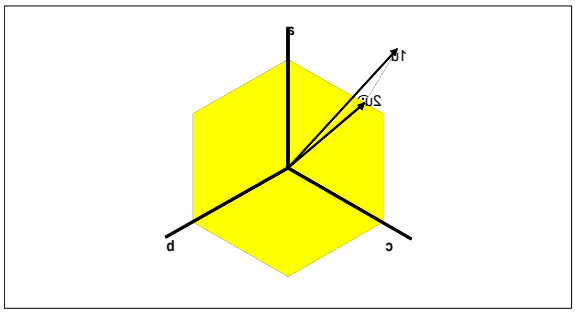

Figure 4: Limiting of the motor voltage

The Current Control

For the digital 3-phase current control a dedicated RISC processor with 20 bit data width and 10 MIPS computing power was designed [1]. The arithmetic unit and the autonomous multiplier perform parallel processing. Special function blocks accelerate the calculations and enhance the quality of the control. The control algorithm is stored in a mask-programmed ROM (20 words of 6 bits).

The current controller is a high-speed, on-line parametrizable digital PI vector-controller with emf compensation and anti-wind-up properties (Fig. 5).

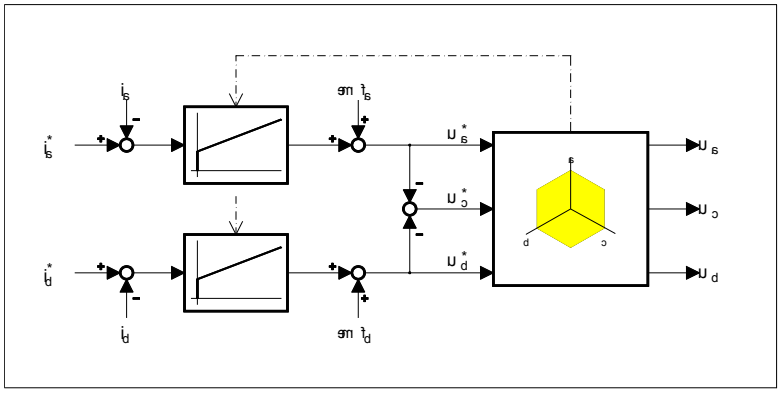

Figure 5: Motor current control with ND32xx

Measuring Circuits

The potential chip is furnished with eight analogue inputs. They enable the measurements of the motor currents, the DC bus voltage as well as the temperature of the transistors and of the motor. Current feed-back signals are measured with a resolution of 11 bit. For the other values the accuracy of 8 bits is sufficient. All measured values are transferred to the periphery chip via the serial bus. The current and voltage signals are, however, processed direct on the chip, too (current and brake chopper control).

The Brake Chopper

The programmable digital brake controller supervises the DC bus voltage. When braking, the motor acts as a generator, converting mechanical energy into electrical one. The electrical energy is stored in the DC bus capacitor increasing thereby its voltage. The bus voltage must not exceed a given critical value. Should it happen then the brake transistor will be activated and the recuperated energy will be converted to heat in the brake resistor.

Timing and Synchronization

Both the potential and the periphery chip, are equipped with their own quartz clock generators of 20 MHz. That of the potential chip is synchronized to the periphery chip by means of the serial data bus. The basic timing of the chips has a common period of 102.4 µs. In order to avoid asynchronous interferences all internal functions of the chips are organized in synchronism with it (data bus, resolver converter, velocity controller, current controller, modulator, brake chopper, etc.). For the supervising computer it is also possible to keep the clock generators of several drives in synchronism.

The Watchdog

This guarding circuit supervises the continuity of the operation of the clock generator and the serial data bus. If there are no telegrams at all received on the bus or a number of subsequent telegrams cannot be evaluated because of CRC fault then it disables the power transistors of the inverter and the brake chopper.

THE PERIPHERY CHIP

The periphery chip ND31xx controls and supervises the information stream between the microcontroller and the potential chip as well as peripheral units (additional memory, CAN-controller, LCD-display). The chip comprises functional blocks for position measurement and feed-back, for torque computation as well as for monitoring the power electronics (Fig. 6).

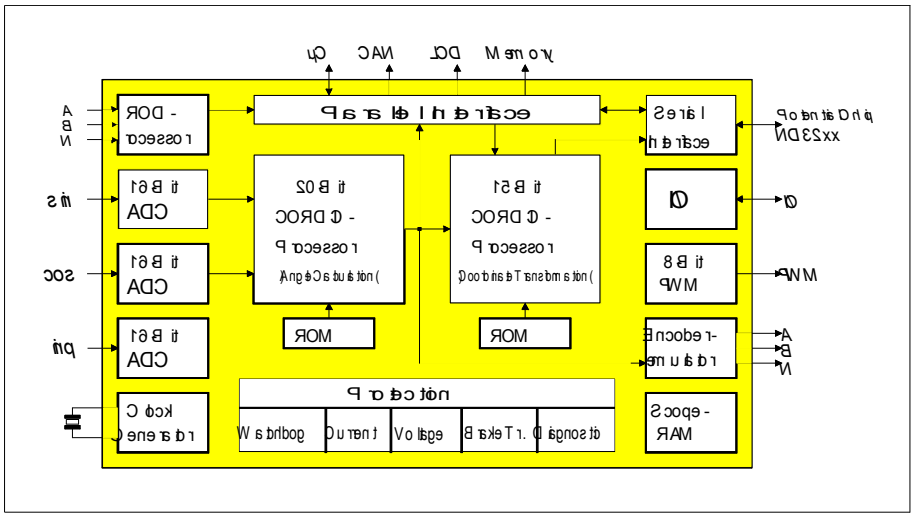

Figure 6: Periphery chip ND3105

The Resolver Converter

The dynamic properties and the accuracy of a servodrive are determined first of all by the quality of the measurement of the position and the velocity. For brushless servodrives these tasks are mostly done by resolvers or optical incremental encoders. A resolver is a robust electro-mechanical transducer. It generates two AC voltages proportional to the sine and the cosine of the rotor angle, respectively. The evaluation circuitry computes from these signals the velocity and the position. In order to achieve a good quality of the controlling a resolution of minimum 14 bits, better 16 bits is necessary.

Tracking resolver converters are expensive. At high r.p.m. they can only produce a resolution of 12 bits. For this reason a dynamic switching of the resolution has to take place depending upon the velocity. This incurs additional complicated circuitry. The maximum resolution and accuracy of digital resolver converters is limited by the quality of the A/D conversion. If this is 12 bits then the position resolution may have at maximum 14 bits. Further if the signals are sampled only once per period [2,3] then determining the position will be very sensitive even to minor interferences. This is why the ND3105 is furnished with high resolution A/D converters which sample the signals 200 times per period. The signal amplitudes are computed by phase sensitive digital demodulator circuits.

The CORDIC Processor

CORDIC processors (*Co*ordinate *R*otation *Di*gital *C*omputer) are special computing circuits optimized for coordinate transformations and for the solution of other trigonometrical equations [4]. So they can calculate the angle based upon sine and cosine values. Since they can do it without requiring clumsy and expensive multiplying circuits (Fig. 7), they are especially suitable for building digital resolver converters. For the resolver converter with a resolution of 16 bit a 20 bit CORDIC processor has been designed with a clock frequency of 10 MHz [5].

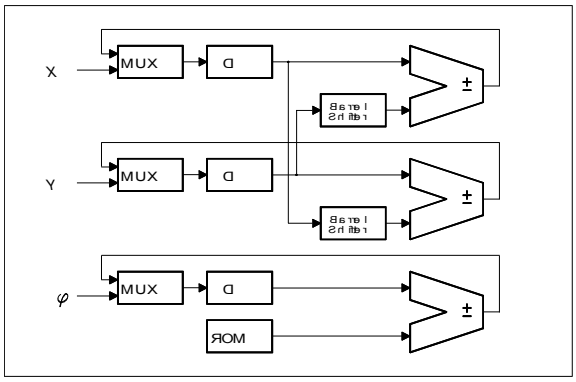

Figure 7: Simplified structure of a CORDIC processor

The Encoder Interface

Another choice for position and velocity measurements is employing optical incremental encoders. To interface such signals the chip contains a dedicated 22-bit processor (*ROD Processor*) which computes the rotor position. The number of encoder pulses per revolution is free programmable. Interpolation of high resolution sine wave pulses is also possible, as well as commutation with hall sensors or absolute tracks.

The *Encoder Emulator* converts measured position values into encoder-pulses for external position loops. The position measurement can be taken from resolver or encoder. The number of pulses per revolution is programmable.

The ROD processor can receive pulses as command (stepper motor emulation). Together with the encoder emulator it is easy to implement a master-slave connection between two servodrives. This is a simple way to realize synchronous operation or programmable electronic gearing.

Field Oriented Control

To realize field oriented control, coordinate transformations have to be carried out. However simple they are, they must be calculated frequently and, therefore, a software solution is time-consuming. Since CORDIC processors can do this chore quickly, a second one, too, with 15 bits resolution has been integrated into the chip as a coordinate transformer. This way the microcontroller of the servodrive could be relieved considerably. Fig. 8 shows how velocity control for a brushless drive can be done using the periphery chip.

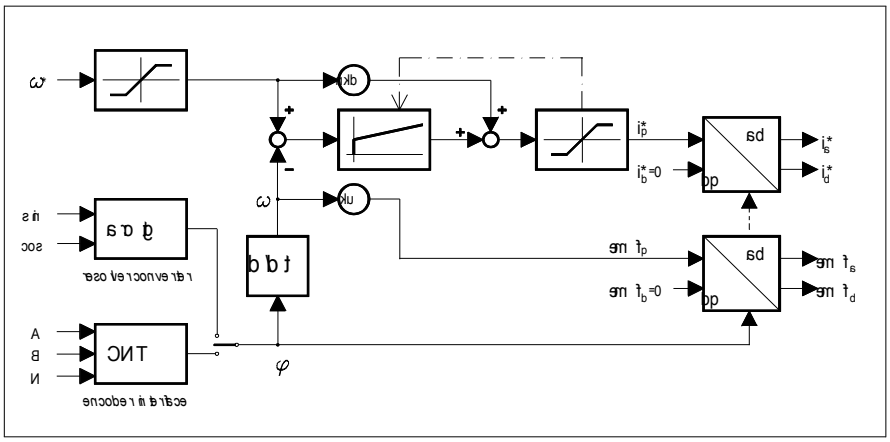

Figure 8: Speed control of brushless servodrives with the periphery chip ND31xx

Microcontroller Interface

There are over 100 registers in the periphery chip dedicated to data exchange with the external microcontroller. Read and write operations are synchronized with the internal clock. If necessary, a double buffering takes place so that even continuously changing data (e.g. those of counters) can be read and written correctly.

Some logic circuits in the periphery chip serve as coupling elements between the microcontroller and other peripheral units such as RAMs, EEPROMs, CAN interface, LCD controller. A programmable wait generator enables cooperation with slow peripheries and it even checks the acceptance of the generated wait-signal by the microcontroller. Another circuit performs simple memory management for external storage elements. A considerable amount of glue-logic has been integrated into the chip, contributing to the reduction of component count in the system.

The CAN Interface

The periphery chip contains auxiliary interface logic between the supervising microcontroller H8/330 and the CAN controller chip i82527. It generates chip-select, read/write and clock signals for the i82527 as well as a wait request for the microcontroller if the CAN controller is addressed. The number of wait cycles is separately programmable for the write and read operations respectively. This enabled interfacing the i82527 without external components (Fig. 9).

It is planned for the next version of the chip set that the i82527 will be replaced by integrating the CAN controller module of IMS into the periphery chip.

IMS has already experience with CAN. First a robust bus driver with overvoltage protection was here developed for CAN bus applications in the automotive industry [6]. The device could withstand voltage spikes up to 120V and any kind of short circuit. It was fabricated in a standard CMOS process as a

stand-alone off-the-shelf component. It can, however, be integrated into any CMOS CAN controller IC as well.

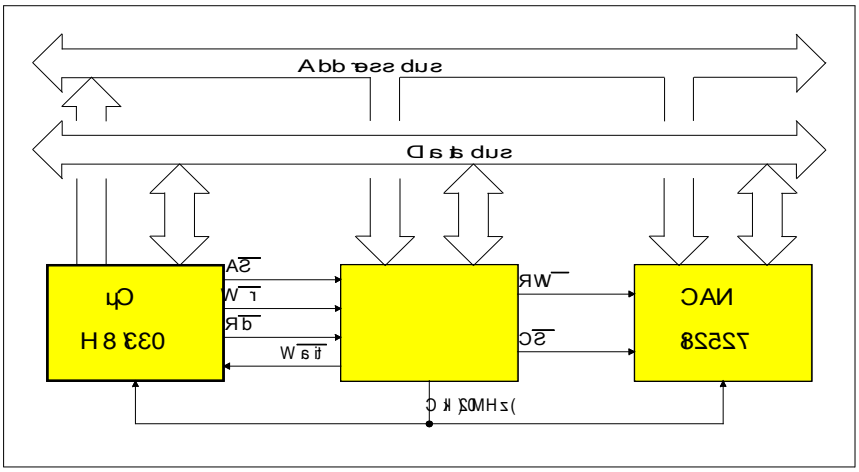

Figure 9: Interfacing the CAN controller

Another CAN-product of IMS is an embedded CAN controller module for ASICs. It is part of a module library for ASICs containing embedded microcontroller. It is at the designers' disposal as a soft macro. The module performs the CAN protocol 2.0 B and has a microprocessor interface with interrupt requests upon events on the CAN bus.

Auxiliary (Input/Output) Circuits

Several auxiliary circuits have been integrated into the periphery chip which can favourably be used in specific individual applications. There is an A/D converter of 16 bit resolution, and a D/A converter built in the form of an 8-bit PWM. If the latter is not used, its output pin can be programmed to act as a one-bit digital in- or output. Similarly the pins belonging to the ROD processor and the encoder emulator are also freely available if these units are not used. Another I/O-pin can be programmed to be a special input for blocking the drive.

Monitor Circuits

The periphery chip monitors the correct operation of the microcontroller and of the potential chip in several ways. A watchdog checks whether the microcontroller keeps sending new data, if not then it locks the modulator in the potential chip. Further it is also checked if the data and address lines of the microcontroller interface stay stable while read and write operations take place. Another watchdog monitors if the communication with the potential chip on the serial bus is confirmed by appropriate acknowledge bits from the potential chip. For diagnostic purposes the number of detected and corrected faults is counted and registered.

Other monitor circuits supervise the current controller and the brake chopper. Overload in the motor

leads, as well as too high or too low DC bus voltage, are detected, reported, and correcting measures are taken. The load on the chopper transistor is also monitored.

Spikes in the serial bus communication and in the lines of the incremental encoder are also detected and reported. Even the surroundings of the chip can, at a certain extent, be checked. By appropriate structuring of the bi-directional pins of the chip, defects on the PCB can be detected (Open leads, short circuits, faulty assembly or defective components).

A 256x8 bit RAM block is contained in the periphery chip. It is used as part of the digital storage oscilloscope function integrated into the drive. This function is very helpful when adjusting the drive. It can also be efficiently used for autotuning or firmware debugging.

THE SILICON FOUNDRY

The chip set was manufactured at the Institute of Microelectronics Stuttgart (IMS CHIPS). As a very economical solution for the chips, the mixed signal GATE FOREST semi-custom family of IMS was chosen [7]. This is a standard 0.8µm CMOS sea-of-gates technology, basically digital but offering some analogue features too. Prototyping costs at the IMS are significantly reduced by using a maskless procedure based upon electron-beam direct-writing technology [8].

For the very purpose of the chip set ND30 an analogue comparator has been developed which enabled the realization of different A/D converter circuits. The chips were designed at the IMS in close cooperation with the contractor Novotron. Schematic entry and simulation were done with *CompassTools*. For automatic placement and routing *Gate Ensemble* was used. Testability was considered during the design. The test was based upon functional verification stimuli with data logic exercises added. The test sequence was graded by fault simulation with *System Hilo*, the fault coverage is 97 per cent. The potential chip ND3202 contains 31000 active transistors and is placed in a PLCC44 package. The periphery chip ND3105 contains 106000 active transistors and is placed in a PLCC68 package.

PRACTICAL APPLICATION

The first application of the chip set is the servodrive Novodrive ND31 by Novotron, a highly dynamic, intelligent brushless AC servodrive. Very good performance has been experienced, especially the qualities of the integrated resolver converter and of the current controller are impressive. The manifold test and diagnostic functions of the chips were very helpful at the development of the hardware, firmware as well as software of the system.

The chip set made it possible to build a complete 2.5 kW servodrive (i.e. control electronics and power stages) on one single 3HE PCB (100 by 229 mm). Resolver converter, incremental encoder input, encoder emulation, CAN- and Novobus-Interface are integrated on the basic board without any additional hardware.

Since the chips undertake much computing chore it was possible to solve many other tasks with an inexpensive 8-bit microcontroller, among others positioning, position control, interpolation and bus communication. ND31 is equipped with battery-buffered RAM. This makes it possible, to download

different CAN communication protocols.
The **first CAN protocol** to be implemented was a customer specific protocol. The aim was to have a very fast and uncomplicated implementation of the protocol. It was optimised to have very fast exchange of command and feedback values with as few as possible communication overhead. In this case command means 16-bit velocity and feedback means 16-bit motor position. It was possible to have command-feedback-exchange for 6 axes within 1 ms. Additional requirements of the protocol are:

- Service channel for parameters and diagnostics
- Slave identification without DIP-switches
- Dynamic identifier distribution

The **second CAN protocol** to be implemented was also a customer specific protocol. It was necessary to adapt ND31 to an existing protocol. Special features of this application are:

- Position loop on the servo drive
- Fine interpolation between the command cycles on the servodrive
- speed up to 22000 rpm
- synchronising several axes

For the future we hope that we can manage to keep the number of customer specific protocols small by implementing the CAN Open Protocol.

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