iCC 1997

4th international CAN Conference

in Berlin (Germany)

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Multi Sensor Controller with CAN Field Bus Interface

Abstract

Smart microsystems reduce the amount of data in field bus systems. A main part of such systems is the Multi Sensor ASIC developed by the Fraunhofer-Institute of Microelectronic Circuits and Systems (FhG-IMS) in Dresden. This ASIC links sensors to a CAN field bus and carries out signal processing tasks. By means of a modular design style on the systems level a good flexibility could be achieved. With its variety of interfaces this ASIC can be applied widely.

Introduction

In classical field bus systems both sensor data are acquired and processed by process computers and control data are transmitted to actuators. The increasing complexity of modern field bus systems requires new net concepts. The intelligence of the single process computer will be shared realising a decentralised intelligence. This is gained by handling the data near the process in the field bus nodes. That way the amount of data to be transmitted is reduced. These smart nodes consist of sensors and/or actuators - the interfaces to processes - a signal processing unit and a field bus interface. Microsystem technology offers good opportunities producing such nodes cost-effectively and tiny. At the FhG-IMS an innovative controller for sensor controlling, signal processing and field bus communication was developed [1]. This controller is the central element of a smart microsystem. An ASIC design on the basis of synthesizable cores was chosen because it has the following advantages over standard IC solutions:

- less costs,
- a higher reliability,
- a shorter development time,
- a smaller system area and
- a better performance. [2]

ASIC Components

As shown in figure 1 the ASIC consists of different components. These were taken from a library of Hardware Description Language cores (HDL cores) and analog macrocells developed at the FhG-IMS. Designing on the top level of hierarchy a flexible, cost-effective and clear architecture could be reached.

The main function of the ASIC is controlled by an *8-Bit-microcontroller core*. It has a RISC architecture and is fully command compatible to MICROCHIP's PIC16CXX. A mapping of existing software is possible with less effort. Simple signal processing algorithms such as range monitoring or the evaluation of the arithmetic mean can be applied. For complex algorithms the integration of a more powerful processor or a dedicated interface to a digital signal processor (DSP) is necessary. Researches referring to this problem were done. The microcontroller core realises a power-saving SLEEP-mode and a Watchdog timer for a reliable operation.

The *analogue cell* consists of an analogue-to-digital converter (ADC), a multiplexer and a reference voltage source. The conversion is based on the charge-balancing principle [3,4] which accounts for high precision at cost of time. Conversion times in the millisecond range can be achieved. For higher frequent conversions other principles have to be implemented. The output word width can be

programmed from 9 to 15 bits by the microcontroller. Two sensors with differential outputs and an output voltage of ± 2 volts (against analogue ground) can be connected to. The ADC can be switched off externally and so the power consumption can be reduced. Additionally, an external reference voltage source can be connected to.

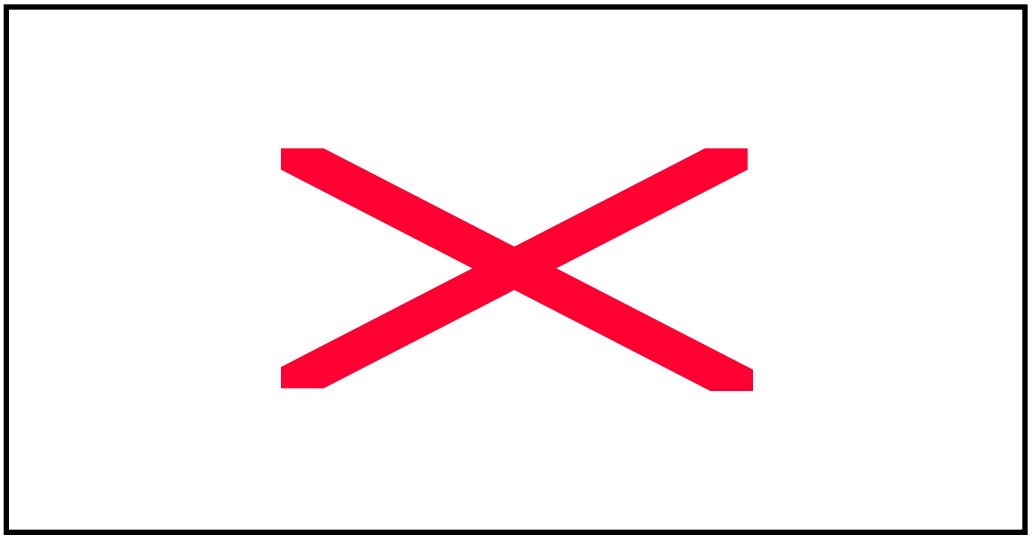

Figure 1: Block Diagram of the ASIC

For the field bus interface a *CAN field bus controller* was implemented. The CAN field bus, which is a multi-master bus, was chosen because it offers the possibility of decentralised intelligence at a minimum of implementation effort. Furthermore, this bus system has an increasing acceptance in the industrial automation and the automotive branch. The CAN interface complies with the CAN protocol 2.0B by BOSCH and the node arbitrates either with the standard or the extended identifier. This interface was designed as a Basic CAN-Standalone-Controller [5]. It is best for microcontroller based chip solutions. In addition, four interrupts decrease the load of the microcontroller core. Data can be transceived at rate of up to 1Mbit per second. The verification of the CAN controller core bases on the test pattern of BOSCH Rev. 2.2/1997. The ASIC was designed that way that the CAN interface can be used separately without the other components.

The *Timer group* generates the different module clocks from the external system clock. The clock rate for the CAN field bus interface can be programmed in five ranges as shown in the table 1 meeting the specifications [6]. A programmable 17-bit counter realises on-chip intervals of 2 up to 500 ms (@8 MHz).

CAN Field Bus clock rate/MHz	Module clock rate/MHz
320 ... 1000	8
160 ... 500	4
80 ... 250	2
40 ... 125	1
20 ... 62.5	0.5

Table 1: CAN clock rates and the related module clock rates

The following *memories* were implemented: a stack RAM (32x13), a ROM (512x14), a RAM (512x14) for user-programme data, a RAM (64x8) as a data RAM and three RAMs (16x8) for the transmission and receive buffers. The RAM and ROM layouts were created automatically using an in-house generator.

An interface with 13 IO-ports to digital components was integrated. Three ports are used to form a three-wire serial interface to external serial EEPROMs. After the power-on reset the user-programme data are loaded via this interface into the internal RAM. Configuration data for the ADC and the CAN controller can be defined and stored in the external memories, too. Otherwise the ASIC will be initialised with default data.

Realisation

The ASIC was manufactured in a 1.0 µm 2-metal-layer CMOS technology. A chip photo is shown in figure 2. The layout of a demonstrator chip has an area of 6,6 x 6,6 mm^2 with a number of gates of 5783 (without memories and analogue components). With further optimisation of the layout the chip area can be reduced by 30%. Experimental results will be presented on the congress.

Figure 2: Chip Photo of the ASIC

Conclusion

This ASIC is a basic part for the decentralisation of intelligence in field bus systems. Sensor signals can be processed near their origin [7]. Process relevant decisions can be made independently from a process computer. The customers needs can be realised flexibly and cost-effectively by means of a modular design of the ASCII with synthesizable cores and macrocells. Because of a consequent description of the circuit with a system description language (HDL) changes of the digital components can be made at less time. Using programmable components ensures a great number of consumers. Interrelated to the hardware design software modules for the microcontroller core were developed for diverse applications and standard routines.

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