Ultimate Product Flexibility & Security by new Flash CAN Controllers

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Abstract

Shortened time-to-market, reduced lifetime and increased product flexibility are some of the attributes of high-tech products requested today. Smart Flash Micro-Controllers with integrated CAN Controller supports these requests by using the CAN bus in two ways:

- **To optimize the control and the communication of the different modules of the application in order to have state-of-the-art functions in a competitive product**
- **To update the customer Flash program memory and the data EEPROM by In-Situ-Programming (ISP), in order to improve easily the customer code or to add new features and parameters to embedded applications in the field.**

The last point requires a strong level of security to avoid any locking situation in the Flash memory up-date procedure via CAN bus initiated in an embedded application.

This paper introduces new low-pin-count Flash Micro-Controllers featuring a powerful combination of Customer Flash Memory, separate Boot Flash Memory, on-chip EEPROM, RAM, 10bit ADC, an advanced CAN Controller and other well selected peripherals. A boot loader and numerous Application Program Interface (API) software support the customer to set-up embedded applications in an efficient way.

Details of these 28-pin (T89C51CC02) and 44-pin (T89C51CC01) microcontrollers part of the new "CANARY" family as well as examples on how it will help to improve system flexibility of a competitive CAN based application, are presented hereafter.

1. Introduction

In today's applications the possibility to alter functions or parameters in the filed is a strong request from the market. This feature, easily usable for the total lifetime of a product, is achieved by the possibility of re-programming a user memory integrated in Flash technology.
Most embedded applications will not allow any work interruption to achieve this update. Furthermore, in most cases the module will not be anymore accessible for the traditional reprogramming on-site, in a factory or in a service center environment, where the programmer is connected directly to the module by a parallel or serial interface.
In applications based on a CAN bus, it is obvious to use this link for ISP in order to provide a suitable and cost effective solution.
To avoid any software crash during the time in which a CAN µController is changing its own application program via the CAN bus, some care have to be taken.
Considering the strong security requirements inherent to CAN applications, "CANARY" offers the following functions:

- Separate User Flash Memory and Boot Flash Memory
- Boot Flash Memory alterable only in parallel mode by programmer
- Boot Control bits in Flash technology
- Default Boot Loader as part of "CANARY" devices which is factory programmed.

2 . Canary Architecture

The T89C51CC01 micro-controller is a member of the TEMIC C51X2 family. This X2 core allows to double the internal execution speed with same external frequency. So, by reducing the crystal frequency of the controller by half, power consumption and EMC are reduced. Extra EMC reduction is also obtained by disabling the ALE signal by software.
T89C51CC01 works at 20 MHz crystal frequency in X2 mode which is equivalent to a 40 MHz Crystal frequency on standard devices.

2 . 1 . Functional Block Diagram

Three independent non-volatile memories are integrated into the T89C51CC01 chip: a 32 Kbytes Program Flash memory, a 2 Kbytes Boot Flash Memory and a 2 Kbytes data EEPROM (Figure 1). This dxevice includes also a 1.2 Kbytes RAM.

The CAN bus is controlled by a powerful CAN controller including the CAN2.0A/B core and a unique programmable mailbox buffer of maximum 120 Bytes.
Added to these features, the micro-controller provides a set of peripherals such as a five channel Programmable Counter Array (PCA) including a Pulse Width Modulator (PWM), high-speed output, timer/edge capture and watchdog function, a full duplex UART, three 16 bit Timers, a dual Data Pointer, five ports with 34 I/Os, a 14 sources – 4 levels interrupt controller and a separate 21 bits Watchdog.

2 . 2 . CAN Controller Functions

The T89C51CC01 2.0A/2.0B CAN Controller handles 15 independent communication channels where each channel can be dedicated to some of the five following functions :

- Reception channel
- Transmission channel
- Receive buffer channel

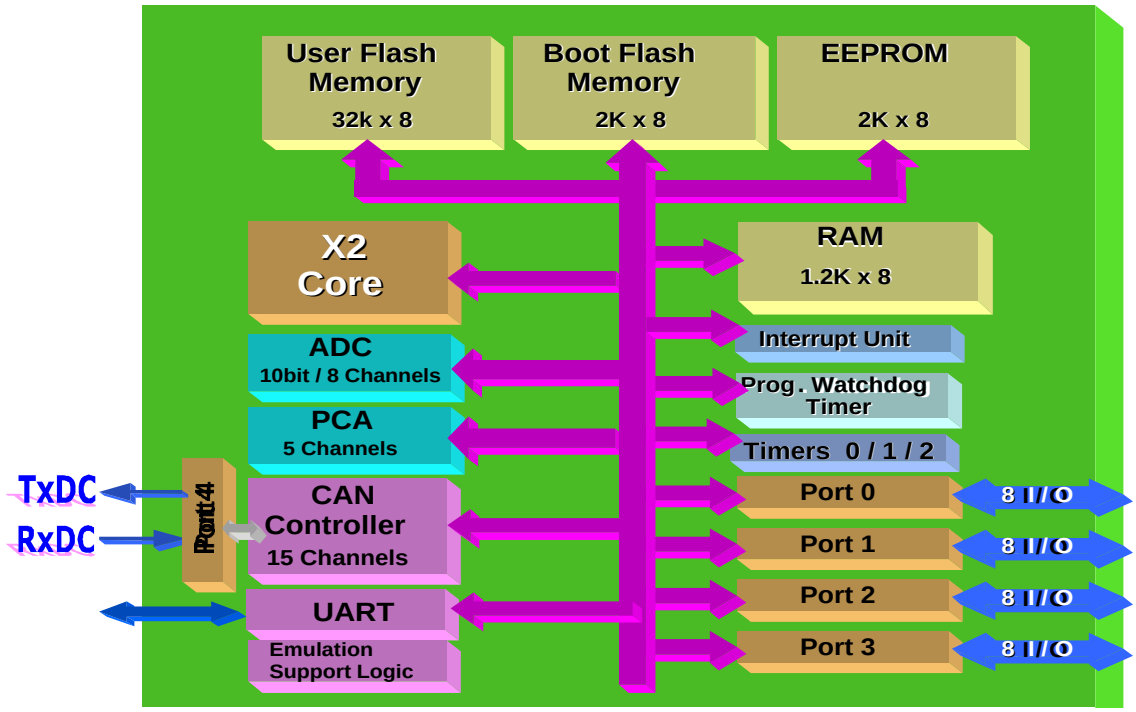

Figure 1 : T89C51CC01 Block Diagram

In order to allow communication with the analog world, a 10-bit, 8 channels Analog Digital Converter (ADC) is also implemented.

- 2.0A or 2.0B mode
- Disable

Each channel can be part of the 120 Bytes Receive Buffer, even in a non-consecutive sequence. All these buffers may be allocated dynamically to one or several channels. Priority in Reception and Transmission is always given to the lowest channel number.
A 20 bytes wide register is associated to each channel:

- 8 byte data
- 4 byte ID Tag
- 4 byte ID Mask
- 2 byte Time Stamp
- 2 byte Status, Control & DLC

A pagination system including 34 SFRs (C51 Special Functions Registers) allows easy access to all the 300 byte (Data 120 byte & Control 180 byte) of the CAN controller registers. All actions on the channel window SFRs are reflected to the corresponding channel registers (Figure 2).
The T89C51CC01 CAN Controller functions are allocated dynamically and can be changed on the fly. This allows to adapt the channel function to the actual application requirement.
In addition to this powerful set of channel functions, the T89C51CC01 CAN Controller supports

- Self Test Mode
- Listen Only mode
- Readable Error Counters
- Error Capture
- Auto Baud (Hot-Plug-In)
- Automatic Reply after reception of Remote Frame
- Time Triggered Communication
- Single shot transmission (no repeat in case of transmission error)
- 16 bit CAN timer with Int at overflow
- 16 bit Time Stamp Register per Channel
- Time Stamp Register trigger at EOF or SOF.

2 . 3 . CAN Controller Handling

After selection of the channel by the CANPAGE register all parameters, identifiers and configuration data are transferred from the SFRs to the corresponding channel registers. Each write or read access to the Message Data Register will auto-increment the mailbox pointer. An access to a pre-selected data byte is possible by locking the auto-increment mechanism and pre-setting the mailbox pointer, also located in the CANPAGE register.

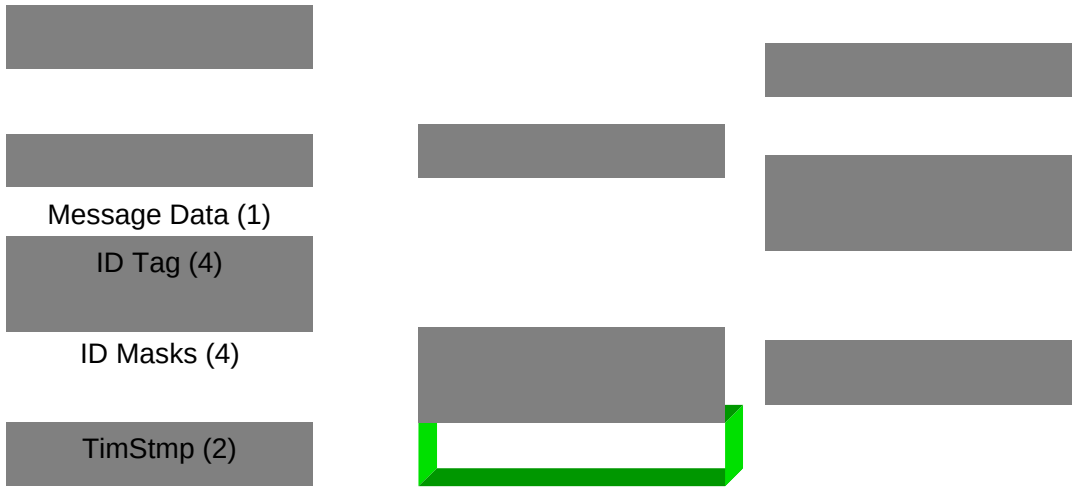

Figure 2 : CANARY CAN Controller mail box concept

The mailbox includes a standard RAM dedicated to each channel. In most cases, it's not necessary to transfer the received messages into the standard memory. Most calculations or tests can be executed in the mailbox area. The
messages to be transmitted can also be built directly into the mail box.
Multi-frame messages can be received easily by using the receiver buffer mode on several channels (up to 15). The frames with an identical identifier will be stored in the reserved channels using an incremented order. Whenever a message is longer than the programmed buffer size, an interrupt is generated. By using an independent receiver channel with the same identifier on a higher channel number, no data may be lost (Figure 3).
A set of API are available in order to handle the interactions between µController and CAN Controller.

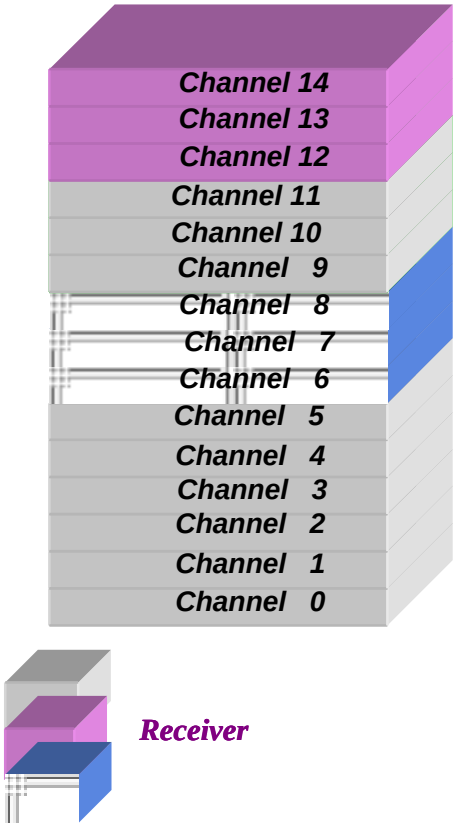

Figure 3 : Example of Channel Data Buffer Configuration, each Channel dispose 8 Bytes.

3 . ISP On-chip Functions

In order to improve system security and to reduce overall application size, T89C51CC01 has three on-chip non-volatile memories (Figure 4.) :

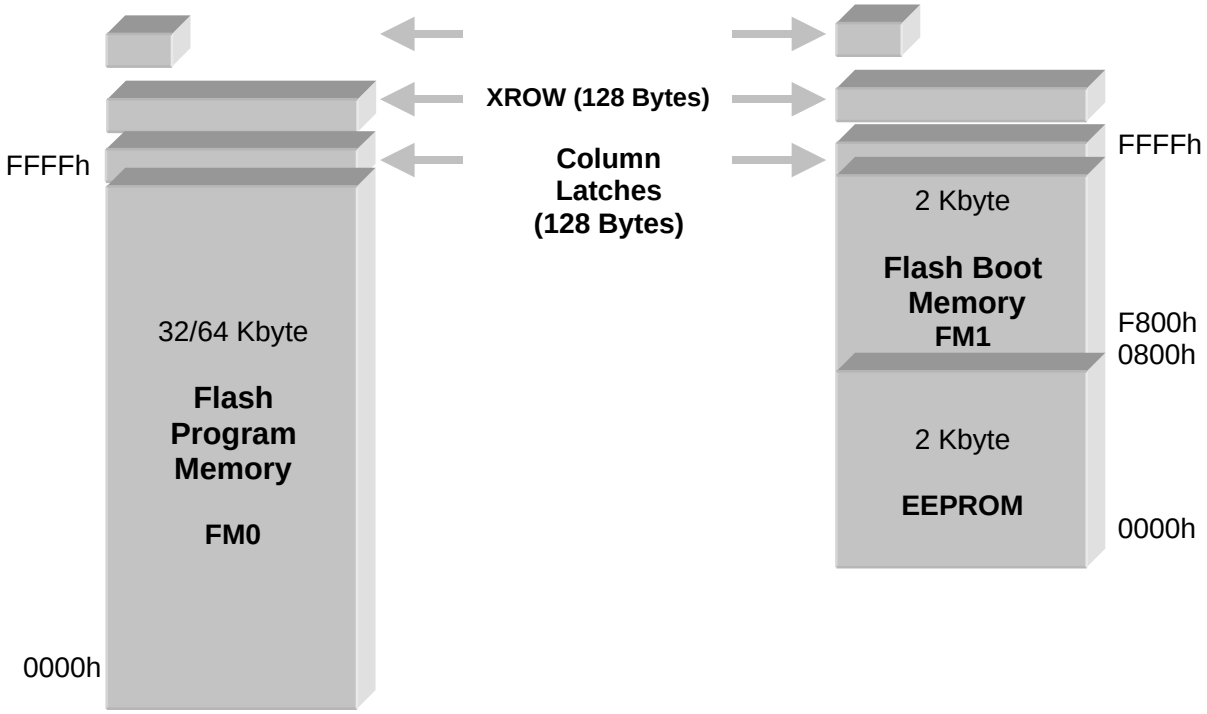

Figure 4 : CANARY Non-Volatile Memory Architecture

- Flash memory FM0 containing 32kByte of program memory
- Flash memory FM1, 2kByte for boot loader and Application Program Interfaces (API)
- 2kByte EEPROM for application parameter storage.

FM0 and FM1 are made of four blocks:
- Memory array
- Extra row (XROW)
- Hardware security byte
- Column latch register.

The column latches contains the input buffers for the three memory blocks. XROW and Hardware security byte are used for FM0 and FM1 read/write (ISP) operations. The 4 MSB of the security byte can be read and written by software, the 4 LSB are readable only by software and are altered by the programmer in parallel mode. Three bits are used to secure the FM0 and FM1 contents against unauthorized access.

For security reasons, the boot memory FM1 can be written only in parallel mode by a programmer whereas the program memory (FM0) and the EEPROM can be altered in parallel mode and by the serial interfaces such as CAN and UART in embedded applications (ISP).

3 . 1 . ISP Programming

To ease and to speed-up the development of T89C51CC01 applications FM1 will contain beside the boot loader, all needed APIs for working with the non-volatile memories (ISP-CAN Protocol). However the customer has the possibility to generate his own routines. T89C51CC01 offers the possibility to locate the customer boot loader in FM0 or FM1.
By using a combination of hardware (programmer in parallel mode) and software programmable flash registers in the Hardware security byte and XROW register T89C51CC01 will starts on one of the three memory locations (Figure 5):
- User application (FM0)
- User boot loader (FM0 or FM1)
- Default boot loader (FM1).

Wherever the program was started, the user has the possibility to change during program execution the memories, e.g. to jump from FM0 to FM1 in order to use the APIs.
The default boot flash loader will include, beside the erase block function, the program byte or page, the verify byte or page, the program security lock bit, and also the ISP-CAN or ISP-UART protocol algorithm which programs FM0 by the data bytes received by the CAN or UART frames.
The program memory FM0 is programmable by:
- the T89C51CC01 boot loader, located by default in FM1
- the user boot loader inFM0
- the user boot loader located in FM1 in place of T89C51CC01 boot loader.

4 . CANARY Applications

T89C51CC01 is especially designed for embedded CAN applications that request easy or frequent code up-date:
- Production automation
- Building automation
- Automotive
- Robotic
- Medical & Agriculture applications

In order to fulfill the request on physical dimensions of very smart applications, like sensors, T89C51CC01 will be available in TQFP44 and CA-BGA64 packages.
High volume and low cost applications are requiring a CAN Controller with same functionality like T89C51CC01 but with reduced memory space and CAN channels. Such device called T89C51CC02, the second element of the “CANARY” family, will be available in a SOIC28 and TSSOP28 package.

State-of-the-art development tools like software simulator, emulators, starter-kit, programmers, binary code of boot loader and API will considerably shorten the Time-To-Market.

5 . Conclusion

With the “CANARY” family, TEMIC Semiconductors provides a new generation of CAN micro-controllers. Based on the popular C51 architecture, these single-chip micro-controllers family include a unique, powerful CAN2.0A/2.0B controller.
The most innovative feature of the “CANARY” family is its set of three independent non-volatile memories which allow data and code up-date via CAN or UART interface with a high degree of system security.
These features provide to the System Engineer the basis to design new and competitive products with an outstanding flexibility.

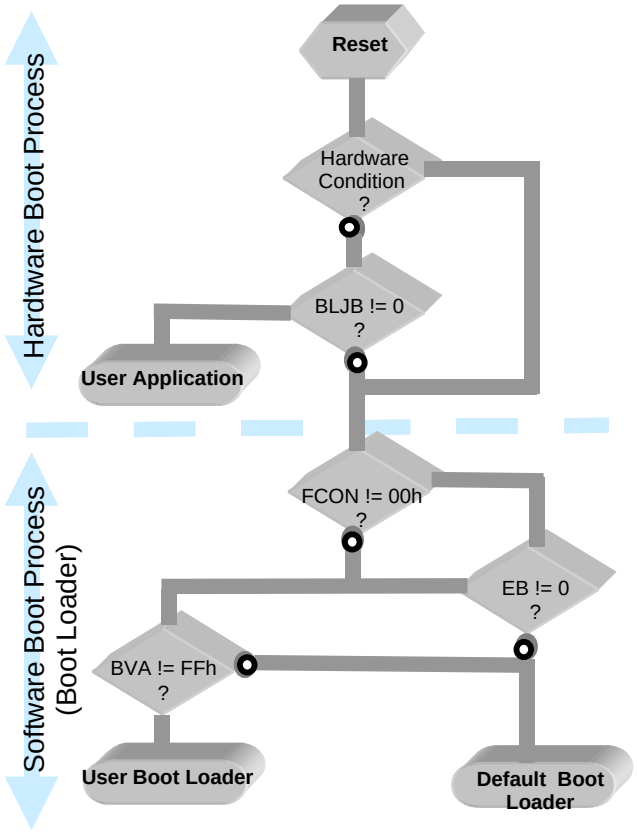

Figure 5 : Example of Memory Selection Algorithm

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