Evaluation and Comparison of the Real-Time Performance of CAN and TTCAN

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This article compares CAN with TTCAN (Time Triggered CAN) by hand of their ability to react to asynchronous external events. For the evaluation the method 'Distinctness of Reaction' is utilized which is based on an orthogonal Walsh correlation. The method measures the average latency response time and the jitter when reacting to asynchronous external events. Furthermore, the measuring procedure yields the 'frequency response' of the communication system which allows the detection of its characteristic properties. Based on the results, a discussion is carried out which enables the derivation of interesting clues in order to plan and optimize time triggered systems.

1 Introduction

Modern control concepts in the automotive field such as X-by-wire or global vehicle dynamics control strategies require highly dependable architectures. Since for the mentioned applications fault-tolerance behavior and determinism is of great importance, time triggered (TT) concepts are expected to be superior compared to event triggered (ET) concepts. The distinction between TT and ET systems is possible by means of the operating system as well as the communication bus, whilst this paper focuses on bus concepts.

The main advantage of time triggered concepts is their deterministic behavior during regular operation, whereas the main advantage of event triggered systems is their ability to react fast to asynchronous external events. A typical example for an event triggered bus concept (and probably the most used one in the automotive field) is CAN [CAN90]. Time triggered bus concept with special emphasis to the automotive field are, for instance, TTP/C [PK98], TTCAN (Time Triggered CAN) [LH02, MFH+02] or FlexRay [BBE+02].

As already mentioned, the behavior of time triggered bus concepts is quasi deterministic during regular operation, since time slices define the permission to access the bus (Time Division Multiple Access, TDMA). Therefore, time triggered concepts provide a higher safety potential, since e.g. missing messages are immediately detected. Other important properties are the possibility to guard the bus against non authorized bus accesses and to realize synchronously working busses in order to take care for redundancy (fault-tolerant systems) [Kop97]. A very important property from the point of view of the automotive field is the so called composability. Since the time slices to access the bus are predefined, the behavior along the time axis is decoupled from the actual bus load. In fact, the predefined phases among the messages are constant. Thus, it is possible to develop different subsystems independently (e.g. by the car manufacturers and suppliers) and subsequently to merge them into the complete system. A comprehensive overview addressing the different properties of TT and ET systems can be found, for instance, in [APF02].

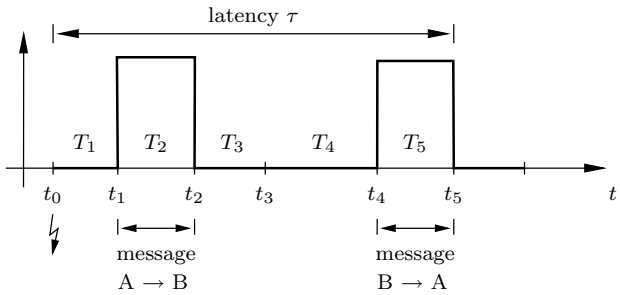
One drawback of time triggered bus concepts is their harder requirements concerning the design procedure, since all processes and their time specifications must be known in advance. Otherwise, an efficient implementation is not possible. Furthermore, the communication and the task scheduling on the control units have to be synchronized during operation, since the different oscillators jitter.

One of the elementary requirement of all real-time systems is their ability to react to an asynchronous event within a predefined period of time. In order to evaluate the quality of the system, the average response time (latency) and its jitter is considered. The main purpose of this paper is to quantify these parameters for communication systems. A comparison of ET and TT busses is carried out, whereas the present comparison focuses

merely on the response to asynchronous external events and neglects other important attributes like fault-tolerance or timeliness guarantees. Obviously, for this comparison ET busses have an advantage over TT busses. Thus, the examination should also show which price one has to pay for the higher safety in terms of the reactivity. This paper is organized as follows:
Section 2 describes the test scenario for the evaluation of the real-time response. Further, the qualitative behavior of ET and TT busses is theoretically analyzed. Section 3 shortly sketches how the measurement is carried out. The utilized method yields the average latency response time and the jitter when a system is reacting to an asynchronous external event. Afterwards, section 3 presents results for CAN (as an example for an ET bus concept) and TTCAN (TT bus concept). Finally, section 4 gives a summary and a discussion.

2 Test scenario

For the following examination the cooperative communication between two control units is considered. The inspected test scenario looks as follows:
A critical situation occurs and corresponding sensor signals reach the control unit A (in the following ECU A). Now ECU A informs another control unit B about the critical situation and waits for its reply. Thus in total the cycle A $\rightarrow$ B $\rightarrow$ A is examined. Figure 1 illustrates this scenario along the time axis.



t_0: appearance of critical situation
t_1: transmission of message by ECU A
t_2: reception of message by ECU B
processing of information at ECU B
t_3: transmission request of ECU B
t_4: start of response by ECU B
t_5: reception of message by ECU A

Figure 1: Test scenario along the time axis and definition of the latency τ

At $t = t_0$ the critical situation occurs and is immediately available to ECU A. The transmission of the corresponding message to ECU B can take place not until t_1. Reasons for this latency $T_1 = t_1 - t_0$ are manifold. On the one hand there is a time demand for the computation at ECU A. On the other hand one has to wait for the permission to access the bus. Subsection 2.1 will explain the different compositions of the latency T_1 for event and time triggered systems. The duration T_2 is the transmission time on the bus which depends on the data rate and the length of the message. The reception of the message by ECU B is finished at t_2. The information processing takes place until t_3. Afterwards, a response for A is required. The permission to access the bus is received at t_4. The scenario ends at t_5 when ECU A receives the response from ECU B.
Since external (environmental) events occur asynchronously, the time at which the critical situation appears is not known in advance. Therefore, T_1 and T_4 are quite susceptible for jitter.

2.1 Origin of jitter

As shown above the overall latency τ is composed of the latencies $T_1, \ldots, T_5$. Particularly, the latencies T_1 and T_4 depend on the bus concept. Therefore, a more detailed examination is carried out for T_1 and T_4.
Figure 2 illustrates qualitatively the behavior along the time axis for an ET and a TT bus concept. The upper part shows a situation for CAN, where the critical situation occurs at an arbitrary instance of time. Particularly, the bus can be occupied if a transmission is currently in progress. Then ECU A has to wait for the next arbitration and receives in the best case the permission to the bus in this next arbitration. The cycle A $\rightarrow$ B $\rightarrow$ A then starts. For this situation to happen it is assumed that the message of ECU A possesses the highest priority compared to all other messages during the arbitration. Summarizing, the following influences are of importance:

- *bus work load and message priority*

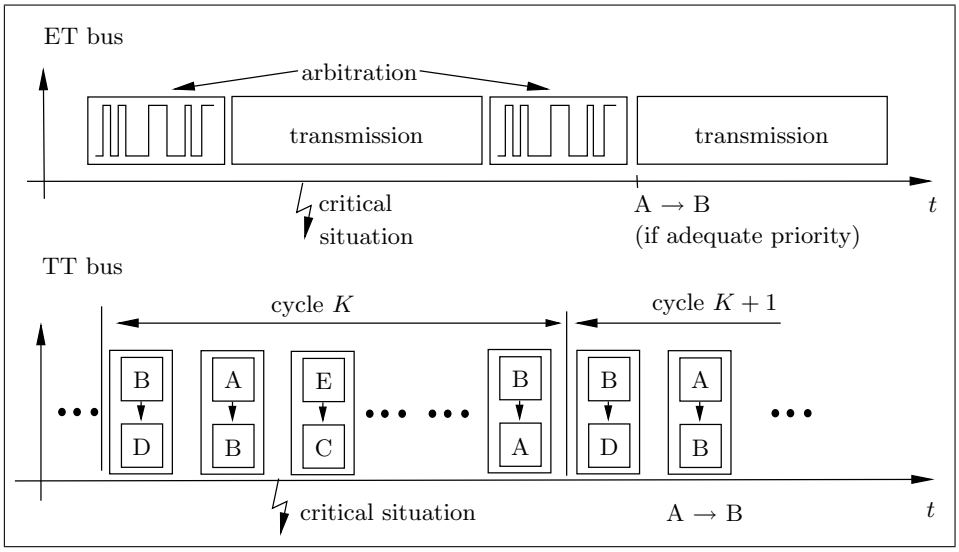


Figure 2: Qualitative response along the time axis for an ET (in this example shown for the CAN bus) and a TT bus

- *maximum length of message and data rate*

The lower part of figure 2 shows the qualitative behavior of a TT bus when reacting to an asynchronous event. For a TT architecture the instance of time at which the message is transmitted in the cycle is well defined. In the worst case, after the occurrence of the critical situation one has to wait an entire cycle, if the respective time slot has just passed. After this idle time it is guaranteed that the transmission will take place. Therefore, for the inspected scenario at least a guaranteed upper bound can be given. Summarizing, the following influences are of importance:

- *cycle structure, cycle time*
- *position and counts within cycle*
- *data rate*

Since TTCAN also allows the definition of free arbitration windows, there is better way to react to asynchronous events[1]. This feature is not considered here, because our aim is to guarantee a clear comparison of ET and TT bus concepts.
If one is concerned to evaluate the real-time performance on the basis of the shown scenario, usually three questions arise:

1.) Does the system react to all critical situations?
2.) Of what magnitude is the average delay τ of the system?
3.) How reliable is the system's response with respect to time? I.e., of what magnitude is the jitter?

To all three questions, the 'Distinctness of Reaction' (DoR) is able to give a quantitative answer [Wol02, WAG03, AWG03].
The method is based on an orthogonal Walsh correlation and yields a reliability measure given by the average latency response time and the jitter when reacting to asynchronous external events. The measurement of the DoR was originally developed for the evaluation and comparison of different real-time operating systems. As presented in [AWG03] it is possible also to evaluate communication systems by this method. Due to lack of space a detailed description of the measuring procedure is not possible in the written paper but will be explained in the oral presentation.
In order to measure the DoR, the communication system is excited by a rectangular signal $i(t)$ of known frequency. This excitation simulates the occurrence of the critical situation. After the described cycle A $\rightarrow$ B $\rightarrow$ A the system reacts in a predefined manner with its response $x(t)$. The signals $i(t)$ and $x(t)$ are processed by a digital circuit, implemented on a CPLD (Complex Programmable Logic Device) which allows to quantify the DoR. For the performed measurements the DoR can take on values from 100% (no jitter) to 0% (at least sporadic loss of excitations).
Not only the determination of a solely value is carried out (constant frequency of the ex-

[1] Besides, CAN in general can be viewed as a subset of TTCAN if the mandatory reference messages are not taken into account!

citation $i(t)$), but the recording of an entire frequency response. A frequency response is known to consist of an amplitude response and a phase response. The DoR determines the amplitude response. The phase response is determined by the average response time τ. In order to achieve a standard of comparison a normalization is carried out and the 'average skew'

$$s = -\tau/T$$

is introduced. The skew s is scaled downwards from 0% to -100%. This choice allows to evaluate the system's quality from the plot by the simple rule

'the higher, the better'.

This rule in the same manner holds true for the comparison by hand of the DoR plots. Further explanations concerning the DoR can be found in the listed literature.

3 Results

This article compares CAN as an example for an event triggered bus protocol with TTCAN which serves as an example for a time triggered concept. The basic differences where explained in section 2.1 and should now be verified by the aid of real measurements.

3.1 CAN

Figure 3 shows on the left hand side the configuration for the examination of CAN. A micro controller board is utilized which is based on the Motorola MPC555 and the real-time operating system RTOS-UH [Ger99]. Since the micro controller itself offers two built-in CAN controllers, there is no need for an extra hardware except the CPLD. Figure 4 illustrates the CAN results for different loads. For all the following measurements the data rate is fixed to 250 kbit/s and the message length equals 2 byte user data. Furthermore, figure 4 also includes a result for TTCAN; the corresponding interpretation is described in section 3.2.
Three load assumptions where examined for CAN:

Scenario Sc1 For scenario Sc1 there is no load. Measuring the time demand for the cycle A $\rightarrow$ B $\rightarrow$ A gives 0.774ms which corresponds to a maximum realizable excitation frequency of 1291Hz. As can be seen in figure 4, the system reaches very closely this limit. This result can also be deduced from the skew which reaches -100%. At this frequency the system reacts exactly at the instance of time of the next trigger. The curve of the skew is nearly linear, which indicates a highly regular behavior. Deviations are due to measurement uncertainties and background functions of the operating system, which are more noticed at higher excitation frequencies of $i(t)$. An example of an essential background function is the timer interrupt of the operating system.

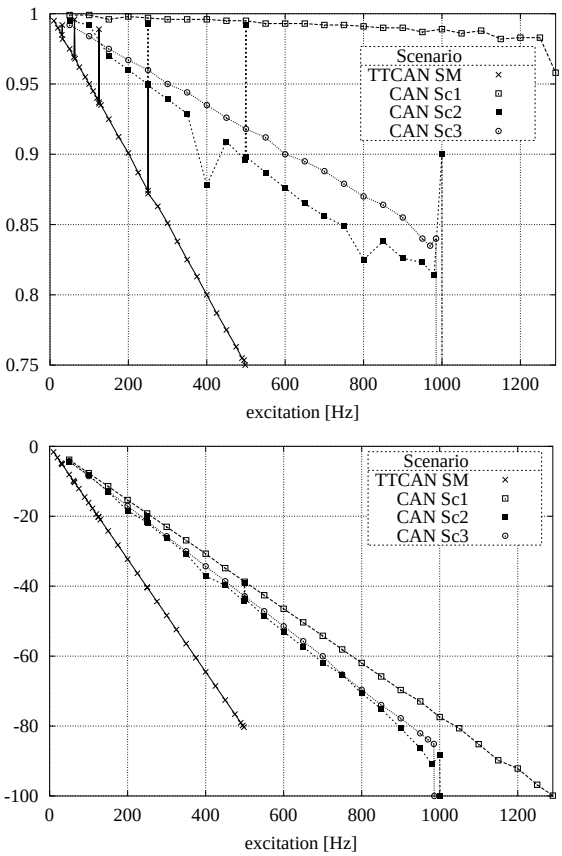


Figure 4: DoR (top) und skew (bottom) for CAN and TTCAN (both at the rate 250 kbit/s).

Scenario Sc2 For scenario Sc2 there is a burden of the bus by low priority messages which are send by CAN node A cyclically every millisecond. There are distinct resonances for the frequencies 250, 500 and 1000Hz (in fact, there are such resonances for every integer factor of 1000Hz, i.e. also for 125Hz, 62.5Hz etc.). The reason for this phenomenon is explained in figure 5. Since background load and excitation frequency are syn-

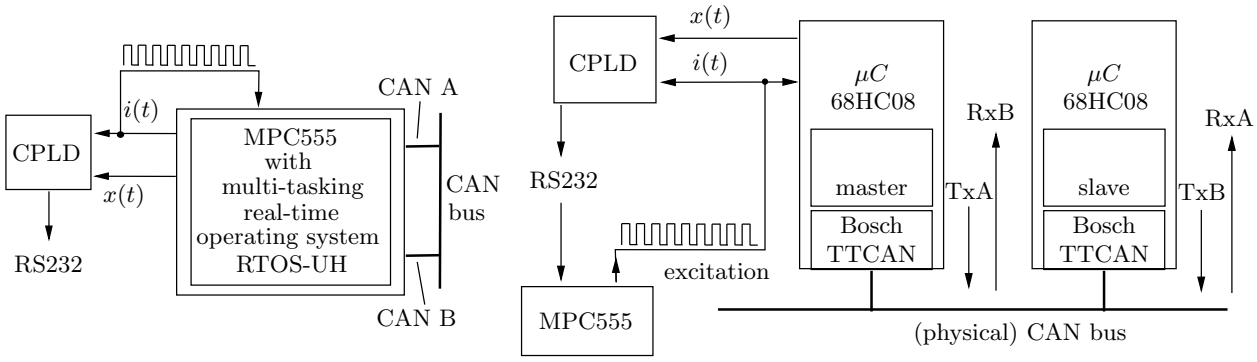


Figure 3: Configuration for the evaluation of CAN (left) and TTCAN (right)

chronous, there is no delay due to the background load and thus there is no jitter.

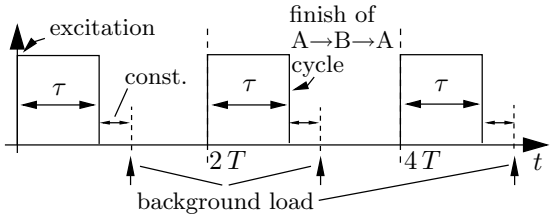


Figure 5: Synchronous background load and excitation

Scenario Sc3 Finally, for scenario Sc3 the micro controller is burdened by its serial interface. For that purpose the interface is parameterized such that an interrupt is generated after the reception of each single character (1 byte). For the serial data rate of 9600 baud and a continuous data stream there is a load of approximately 1000 IR/s. As can be recognized in figure 4 again jitter arise, since the micro controller is interrupted during the processing of the messages of the A → B → A cycle. Thus, not only load on the bus but also on the micro controller generates jitter.

3.2 TTCAN

The right hand side of figure 3 already showed the configuration for measuring the TTCAN bus. The configuration is based on two micro controller boards (Motorola 68HC08). Additionally, stand-alone chips of Robert Bosch GmbH are mounted on the boards. They implement the TTCAN protocol [Har02]. The package of a micro controller board and a TTCAN chip represents a communication node (ECU). One of the nodes represents the master[2] (corresponds with node A), the other node serves as the slave (corresponds with node B). The excitation of the system is performed by the already mentioned micro controller board on the basis of the MPC555. This board also carries out the evaluation of the measurement via its serial interface.

For time triggered bus concepts the communication structure is defined in advance and generally not modified during operation. For that purpose the TTCAN chips are initialized at start-up; afterwards, they operate autonomously. Merely the data of the messages may be modified during operation. Figure 6 demonstrates a simple communication structure with two messages (besides the reference message) in every cycle. This cycle is illustrated from the point of view of the master where double framed boxed mark actions of the master node. Within the cycle at first the message of the slave (node B) is defined and afterwards the message of the master (node A). Thus, from the point of view of the master, the cycle consists first of a receive message and then of a transmission message. In the following this constellation is called the scenario SM. The cycle time equals 1ms which

[2]The master node is a dedicated node of the TTCAN bus which is responsible for the transmission of the so called reference message. All participating nodes carry out the time synchronization with the aid of the reference message. Further information can be found, for instance, in [LH02, MFH+02].

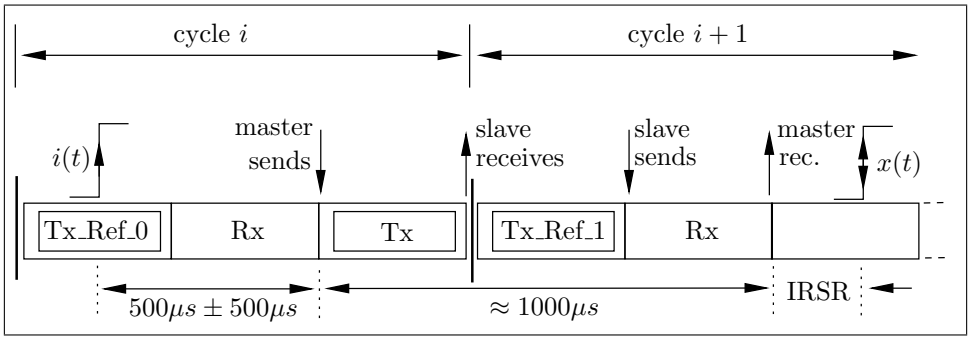


Figure 6: Scenario SM seen by the master and expected latencies

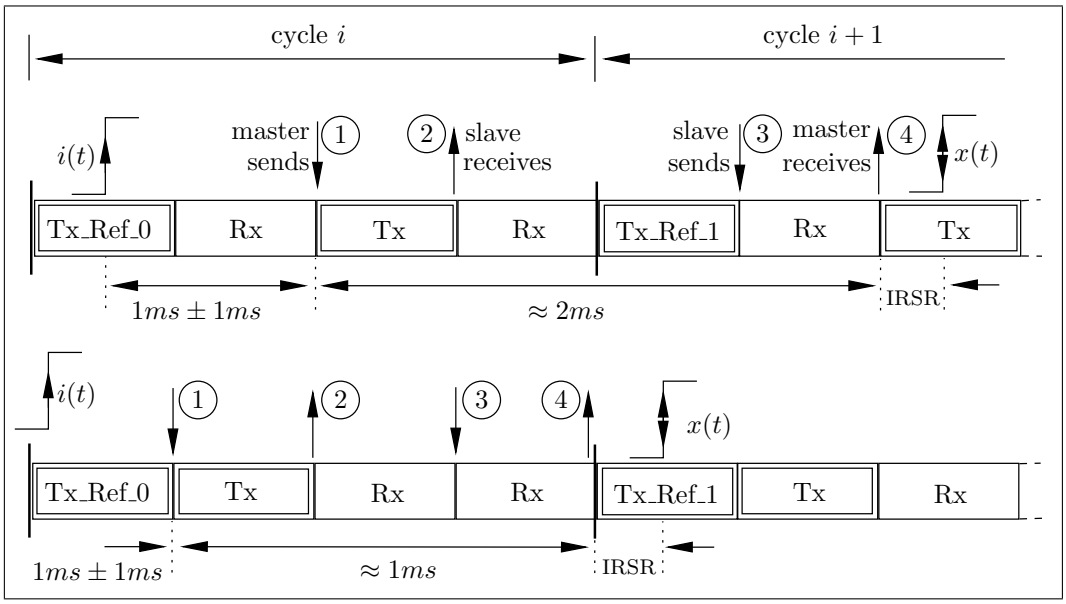


Figure 7: Scenarios SMS & MSS seen by the master and expected latencies. Top: SMS; bottom: MSS.

for the chosen message length gives a bus load of 95.6% if the reference message is considered in the calculation and 66.4% otherwise. The results were already presented in figure 4. As could be expected beforehand, the maximum excitation frequency is 500Hz, since the inspected cycle A → B → A at least requires two communication cycles. Higher frequencies lead to the missing of triggers.
Again resonances are detected but here for every integer factor of 500Hz. At this frequencies the excitation and the cycle structure are synchronous. Both, the DoR as well as the skew show a linear characteristic, which indicates a regular behavior. Figure 6 allows the estimation of the expected latencies for the scenario SM as follows:

- The excitation $i(t)$ can occur at any instance of time within the cycle. Therefore, the average response time of the master equals $500\mu s \pm 500\mu s$.
- There is a demand of an entire cycle until the master receives the answer message. This additionally generates a latency of 1000 μs (corresponds to the cycle time).
- Finally, one has to wait for the completion of the interrupt service routine (IRSR), until the expected reaction at the output $x(t)$ is recognized. (The defined reaction of the system is a toggling of the output $x(t)$. More details can be found in [WAG03, AWG03].)

Neglecting the run time of the IRSR one has to expect in total a latency of

$$1500\mu s \pm 500\mu s \quad .$$

At f =500Hz one could expect an average latency of -1500/2000 = - 75%. The difference to the measured value of -80% is due to the time demand for the IRSR.
Now the cycle structure is modified such that the slave is allowed to access the bus twice in every cycle. The cycle time is set to 2ms which yields a bus load of 64.4% (with reference message), resp. 49.8% (without reference message). For the structure of the communication now three constellations are pos-

sible: SMS, MSS and SSM. Within our studies the scenarios SMS and MSS were further examined. Figure 7 shows both scenarios from the point of view of the master. The encircled numbers show the corresponding actions in both scenarios. Theoretically, for the scenario SMS one has to expect a latency of $3ms \pm 1ms$ and for the scenario MSS a latency of $2ms \pm 1ms$, respectively. At this the assumption is made that the micro controller of the slave is too slow in order to react in the time slot immediately following the time slot of the master's message. In fact, the slave has to wait for the next permission to access the bus. The real measurements of figure 8 confirm this assumption. Although there is an identical bus load and the same jitter behavior (DoR of SMS and MSS), there are different curves for the skew – meaning different latencies. Such effects have to be considered during the design of an adequate communication structure, if one has to assure an efficient implementation.

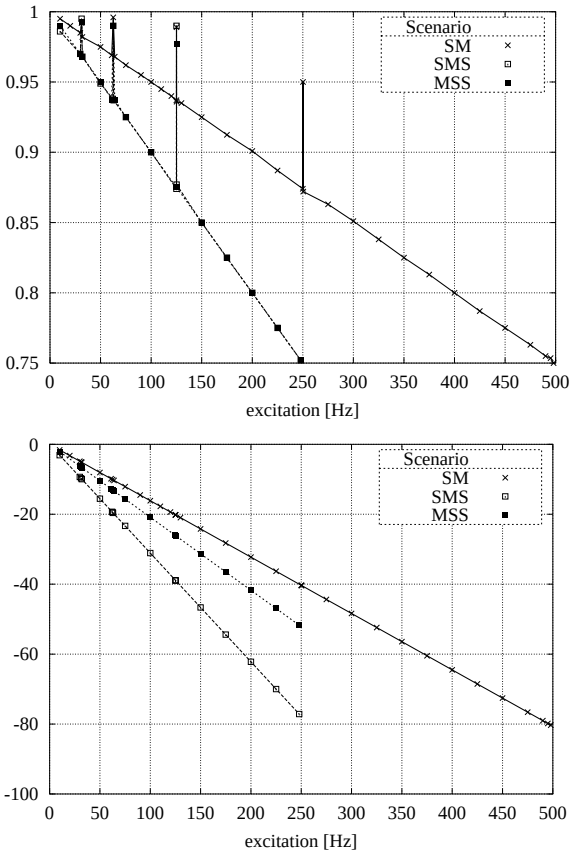


Figure 8: DoR (top) and skew (bottom) for TTCAN, each with the data rate 250 kbit/s. Scenario SM: 1ms-cycle. Scenarios SMS and MSS: 2ms-cycle.

4 Summary and discussion

This article described measurements in order to objectively evaluate the real time performance of bus systems when reacting to asynchronous external events. The results for CAN served as an example for an event triggered bus concept and measurements for TTCAN were carried out in order to evaluate a time triggered bus.

Without any safety mechanisms based on software, for CAN a maximum bus load of 50% is often recommended for not critical applications. For real-time critical applications a maximum bus load of approximately 20 - 30% is suggested in [LH02]. For TTCAN a much higher bus load is realizable (theoretically up to 100%), although some performance has to be dedicated to the bus concept (e.g. for the reference messages). As shown by the measurements, event triggered bus concepts are more efficient for small bus loads, since they allow lower latencies due to their ability to react fast to asynchronous events.

A bus load or a load on the micro controller worsen the behavior of the CAN bus. For TTCAN the result is almost independent of the actual load and the DoR as well as the skew show a linear characteristic with respect to the frequency of the excitation. Thus in a sense, TTCAN is deterministic (compared to CAN), since the limit of the (worst case) time behavior can be determined in advance and is therefore known.

The different scenarios for TTCAN and in particular the comparison of the scenario MSS with SMS has shown, that the speed of the micro controller as well as the concept of the operating system on the micro controller has to be taken into account. This quite simple example already demonstrated that the design of the communication structure in not merely a question of finding the smallest common multiple for given message repetition rates. Furthermore, the order of the messages and the dependencies between the tasks on the micro controllers have to be considered. Under circumstances even the introduction of time waits (gaps) can result in an increase of

the performance in the sense of a higher ability to react to external events.
Generally, the realization of a distributed control system on the basis of a time triggered bus requires an overall design which considers all tasks of the participating micro controllers. The algorithmic search for an adequate solution is not a trivial problem. Under circumstances it is necessary to evaluate situations which are very difficult to be modeled. Such a task is, for instance, the determination of the worst case execution time (WCET) of some routines on the micro controllers. Another example is the partitioning of cooperative tasks on different micro controllers.

Acknowledgement

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