Experiences and challenges of CAN transceivers in up-integrated system basis chips

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This paper will discuss the experiences and challenges with the implementation of up-integrated CAN transceivers found on system-basis chips (SBCs) for the automotive market segment. These SBCs exist in an extremely harsh environment, factors such as system interoperatibility, enhanced electrostatic protection, and electromagnetic interference need to be understood and designed in the integrated component to help reduce issues at system level. This is further complicated as the needs for up-integration forces a less than idea silicon process selection to maintain cost goals for the SBC. Detailed discussion of lessons learned include the silicon process development of ESD robust structures at the device level using a lateral-DMOS silicon controller reticifier; the addition of clamp structures to protect the device during short circuit conditions when a CAN choke is used; the influence of fault protection structures on the robustness of the receiver to electromagnetic interference during direct power injection testing; the future market trends for system-on-a-chip development and the impact of process selection to ensure the feasibility of an up-integrated transceiver; and system power up/down issues to minimize bus distrubances. The paper will conclude with future challenges related to up-integrated CAN transceivers.

I. System Basis Chips (SBCs)

Over the last decade, the automotive industry trend has been to move to highly up-integrated, smart power Integrated Circuits (ICs), also known as system basis chips. Systems previously containing multiple ICs, each providing a specific function, now contain one or two system-on-a-chip ICs containing a wide range of analog, power, and digital functions. Like many ICs today, they have a digital core comprised from a standard cell library similar to a digital application specific IC (ASIC). They also include analog building blocks such as operation amplifiers, comparators, data converters, and voltage/current references. Somewhat more unique is that power circuits are also incorporated into the IC to add the ability to control motors, switches, and solenoids, and to generate power supplies, both switching and linear, for internal and external circuitry. On a single piece of silicon, one can find low power circuitry biased only with few microamperes of current that may be next to a power device switching several amps of current. Figure 1 shows an SBC with several of the building blocks. Note that the CAN transceiver utilizes only a fraction of the die area needed for the IC. Although the transceiver serves an important communications function, the circuitry alone is not sufficient to drive process definition.

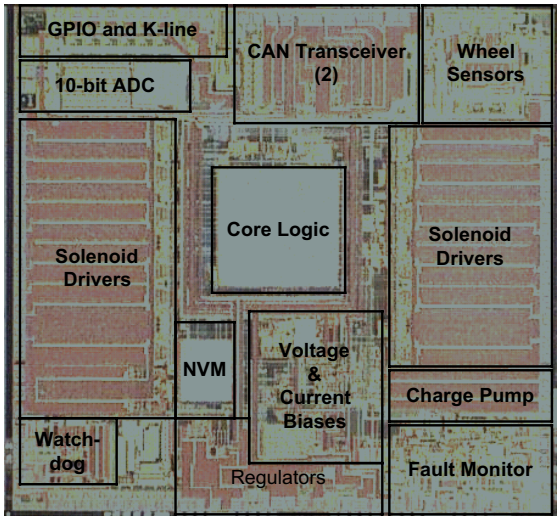

Figure 1: Example System Basis Chip

II. The Challenge

To build an up-integrated CAN transceiver on a highly integrated IC is a challenge as the semiconductor technology that is chosen is not based solely for the transceiver. Higher levels of integration force semiconductor process development engineers to choose fabrication steps and create components that offer higher levels of digital integration with high precision analog devices and high voltage power devices. The addition of power devices also benefits CAN transceiver design as higher voltage components allow the common-mode range specification to be met.

However, the process must also be a low-cost solution. To achieve this goal, a junction isolated process is used instead of the more expensive dielectric isolated process. Junction isolation requires fewer process steps, and is hence less expensive to manufacture. However, dielectric isolation benefits from the lack of active parasitic components which complicate circuit design and often cause unsuspected operation. These parasitic components often become active if the node is allowed to traverse above or below the supplies, thereby forward biasing PN junctions . Furthermore, it is important to realize that these PN junctions can be the base emitter junction of NPN or PNP transistors. Figure 2 shows a CMOS cross-section with the numerous parasitic components that exist.

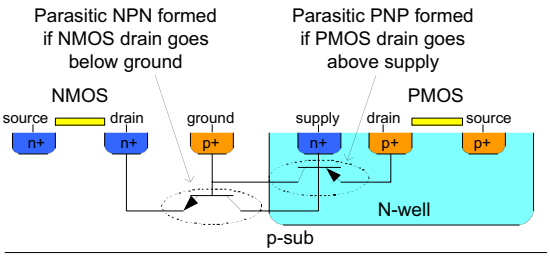

Figure 2: CMOS cross-section with active parasitic components

Regardless of these process technology challenges, the automotive environment requires a robust transceiver design. While needing to meet the ISO11898 standard, additional requirements are needed in the areas of electrostatic discharge protection (ESD) and electromagnetic immunity (EMI). While the standard recommends protection to short circuit faults from battery and ground, as well as shorted load conditions, the use of chokes to improve radiated emissions can cause higher than expected transient voltages along the CAN bus which the transceiver must tolerate without failure.

III. ESD Protection

Insufficient ESD protection on the CAN bus pins is one of the leading causes of failures and device returns. As the bus pins are the means of communication between different modules within the car, it is susceptible to mishandling during assembly or maintenance as the pins are exposed to an unprotected environment.

Although every company quality target is zero DPPM (defective parts per million), automotive companies insist on it. Defective parts can come during the assembly process, initial testing, or field failures. The failures due to ESD exposure must be reduced or eliminated, and increasing protection levels is one of the methods that can be implemented on ICs.

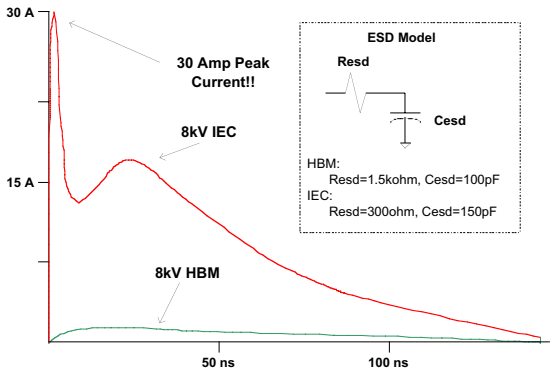

Figure 3: IEC and HBM ESD model comparison.

There are two main models for the ESD event: human body model and the International Electrotechnical Commission (IEC). Although human body is the most familiar to IC manufactures, IEC is more important to system engineers. The IEC strike is much more severe due to the higher capacitance and voltage, as well as the requirement that the strike occur when the device is both powered-on and –off. IEC is presently a focus as it is believed to be representative of actual ESD events in the field. Figure 3 illustrates the differences between the HBM and IEC

ESD model, as well as the transient current waveform for an 8kV strike.

Car makers and tier-1 suppliers (module suppliers to the carmakers) have continued to increase demands on ESD performance. European companies have been steadily increasing performance requirements from 8kV to 15kV over the past few years, with the Japanese manufactures requesting as high as 25kV.

Traditional ESD structures that clamp the output voltage to protect internal circuitry have been tried. However, it is important to keep in mind that for a 25kV IEC ESD strike, it is expected that currents of 45 amps are expected to exist for 50nsec. Although ESD structures are able to handle this amount of energy (<30uJ), it is difficult to create a traditional clamp structure that has sufficiently low resistance to protect the internal circuitry.

The characteristic of a good ESD protection device is a low impedance when conducting under ESD strike, completely inactive during normal operating condition, fast turn on and capability to turn off the low impedance path at the conclusion of the ESD strike. An SCR, if it can be successfully turned off without latch up or other problems in the IC, is a very attractive ESD protection device because of the very low impedance in the on state. This is accomplished by allowing the voltage to "snap-back" once the triggering voltage is reached, enough margin is gained to offset any issues caused by parasitic on-resistance.

The device is built in a bipolar complimentary MOS (BiCMOS) process.[i] The SCR structure is based on the standard LDMOS device with characteristics which have been reported in [ii]. Figures 4a and 4b compares the cross sections of the standard 60V LDMOS device and the new SCR-LDMOS device. As can be seen from Figure 4b, current flowing underneath the drain side p-region can forward bias the p-n junction on the drain side, thus helping trigger the pnpn SCR structure. Details of this structure can be found in reference [iii].

Although this device increased the level of ESD protection, a problem was introduced. One of the major disadvantages with using an SCR structure is that the if the SCR were to fire while the bus was shorted to battery, then there would be no way to unlatch the SCR. Under these conditions, the SCR would be destroyed. This can be protected, but it is then important to understand situations that could cause the SCR to trigger.

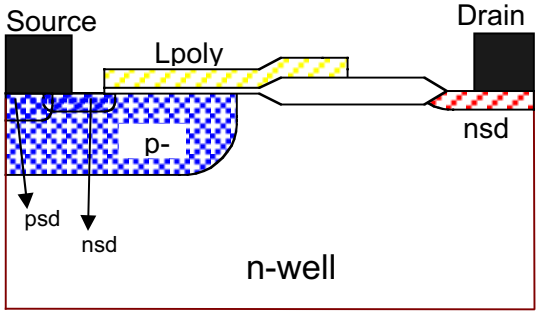

Figure 4a: Standard LDMOS cross-section

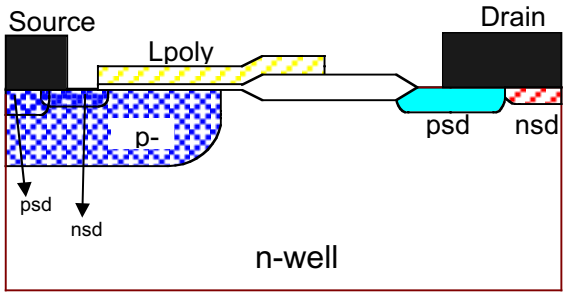

Figure 4b: SCR-LDMOS cross-section

IV. Inductive kicks – another problem

One aspect of the CAN bus that can cause excessive voltage transients is the inductance associated with the wiring under short circuit conditions. Figure 5 shows a system under short circuit conditions and the current circuit configuration to protect against positive voltage transients. As the driver is turned on, CANL goes into current limit, establishing a current in the inductor. When the driver turns off, inductance in the wiring tries to maintain the same level of current and since the CANL node is now high-impedance, the voltage on CANL rises until the energy in the inductor is removed. As the inductance of the line is small, it does not have significant amounts of energy. Traditionally implemented ESD structures are able to handle this transient.

However, if an SCR ESD device is used for protection, then damage can occur as this voltage transient spike will trigger the ESD structure. When a short is applied

from a low impedance source, the SCR will continue to conduct until it is destroyed.

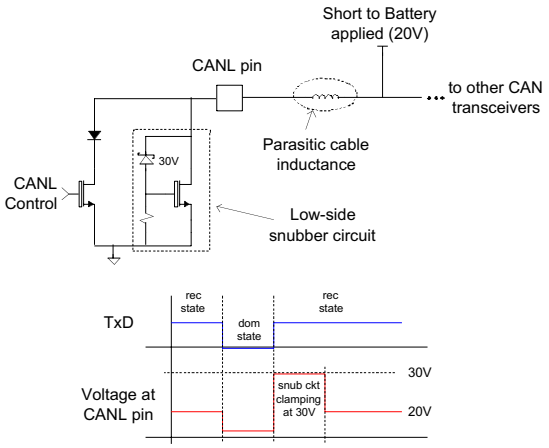

Figure 5: Circuit showing short circuit condition and low-side snubber circuit to prevent voltage transient.

To solve this problem, a low-side snubber circuit is used to limit the voltage on the CAN pins. The IV characteristic of this circuit is much like a diode, except that the forward voltage is much higher. Care needs to be taken in designing the clamp to account for process and temperature variations of both the forward voltage of the snubber and the triggering voltage of the ESD structure. The forward voltage of the snubber always needs to be lower than the ESD triggering voltage.

V. CAN Chokes

In some systems, CAN chokes are required to both minimize radiated emissions, and improve the immunity of the receiver. The choke is best described as a transformer using in-phase windings. During the dominate state transition, the choke attempts to match the currents coming out of CANH and going into CANL. This provides as much symmetry as possible for the current waveform, and hence preserves the common-mode voltage signal as measured at the mid-point of the termination. For noise that is coupled on to both CANH/CANL, the choke acts as a filter to remove the common-mode component of the signal. Any currents that are flowing from the bus to the transceiver pin are cancelled as their magnetic fields within the transformer are equal and opposite.

Unlike the bus wiring, the CAN chokes are known to have inductances as high as 100uH. This requires that the snubber network needs to be designed to handle this energy.

So far, we have only discussed the CANL pin. The CAN choke is a transformer, and hence changes in current in one of the transformer windings can affect the current through the other. Figure 6 illustrates the condition where a 20V short condition occurs along the bus side of the choke. When the driver goes into dominate state, the current builds up in the choke on the CANL side. As most transceivers are designed with a current limit, this part of the waveform does not pose any problems for the device.

However, upon entering recessive state, the CANL pin starts to transition positive as the current in the transformer cannot immediately change. The voltage increases to a point where the polarity across the transformer is changed, at which point the current begins to decay. However, this change in current is mirrored in the other winding which raises the voltage on CANH. Under these conditions, it can be shown that the change in voltage is approximately equal for both CANH and CANL. The problem is that CANH begins at the short circuit voltage (in this example, 20V). If CANL is allowed to rise to 30V as dictated by the snubber network, then CANH will also rise to 30V resulting in a final voltage of 50V. This voltage is beyond the ESD triggering voltage, and must be lowered.

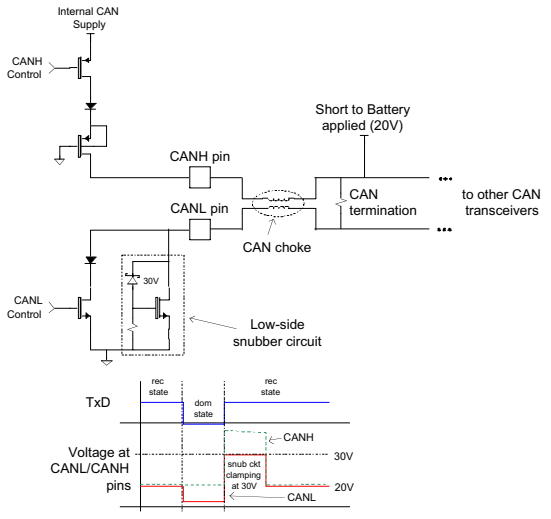

Figure 6: CAN short circuit with CAN choke

The solution to this issue is to provide an additional snubber network on the CANH

pin as well. Although the amount of energy needed for the CANH winding is much smaller, it is important to keep the electrical matching between CANH and CANL for good signal quality.

VI. Electromagnetic Immunity Testing

It is difficult to translate noise/coupling sources in the car to something that the IC designer can use to design/simulate a robust transceiver. The current focus for Tier1 and SBC developers is the Direct Power Injection (DPI) test which is used as a gauge of the robustness of a CAN transceiver in an automotive environment.

A brief overview of the DPI test is shown in figure 7. A RF power amplifier is used to inject a common-mode AC signal onto the CAN bus during transmission and the RxD output of the transceiver is monitored for any glitches or jitter based upon the RxD mask. This signal frequency ranges from 1 MHz to 2 GHz, and input power is as high as 36dbm. However, as the impedance of the CAN bus is not constant, this signal could range from 28 Vpeak for a 50 ohm termination to 56 Vpeak for a high impedance load.

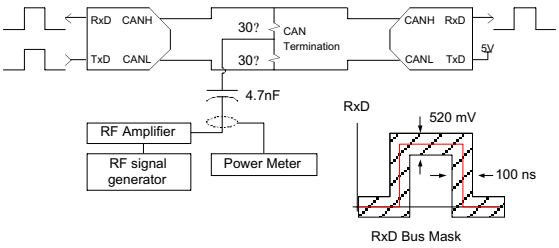

Figure 7: DPI test steup and RxD bus mask.

To achieve this level of performance, it is not necessary to increase the common-mode voltage range of the receiver to +/- 56 Vpeak. However, it is important to maintain dominate or recessive voltage levels during the DPI test. For dominate mode, this is normally not a problem as the driver will provide a low impedance path to either the supply or ground. This will keep the bus in a dominate state.

For recessive state, the CAN bus pins needs to be matched as closely as possible to prevent the generation of any differential mode signal. Care must be taken that this be done for both DC and AC cases.

Although dominate state appears to have less concern during the DPI test, there is a concern with the tripping of over-current detection signals. For SBCs, fault reporting is required to inform the module of communication issues. If a short circuit fault occurs, specific actions are taken which may include discontinuing communications. Given the high voltages that are being injected on the bus, it is quite possible that the over-current fault be triggered. To eliminate this occurrence, both analog and digital filtering is used to distinguish between a true short circuit fault and coupling from a radiating emissions source.

VII. Interoperatability Issues

Normal operation of the CAN bus is well understood. However, complications arise during the up-integration of a transceiver onto a more complicated device, as well as demands from customers to make the transceiver as robust as possible.

One example of an interoperatability issue occurred during power-up and –down of the system or module. The SBC shown in figure 1 is powered from the car battery, and then internal supplies for logic, analog, and the CAN module are generated. However, if the CAN transceiver section receives it's power prior to the logic, the CAN can be inadvertently be driven into dominate mode, and pull down the bus during power up sequencing.

SBCs are custom devices, and are subject to additional specifications beyond IS018949. For example, faster loop times are being requested to minimize the affects of wiring associated delays. This usually requires some active circuitry to assist with the dominate-to-recessive state transition. The concern is during arbitration the bus may be pulled to a recessive state momentarily during the transition. Again, care must be taken that this circuitry does not affect bus while performing its task.

Another issue that has been experienced is the loss-of-ground condition. Under these conditions, the ground of the module is disconnected from the chassis while the battery connection is still maintained. Current paths through the module and the

SBC will pull the module's ground towards the battery supply voltage. However, the CAN bus pins will continue to be referenced to the chassis ground, and appears as a very negative voltage with respect to the SBC ground. As the battery voltage can be as high as 40V under load dump conditions, there have been requests to design the CAN bus pins to traverse as far as -40V and remain high-impedance so as not to allow any current paths under these conditions.

VIII. Future Direction

The ultimate CAN transceiver is one with no emissions, infinite immunity to emissions, high speed, and low cost. As process development continues towards higher integrated solutions, and eventually true system on a chip IC will be developed where microprocessors, analog, and power circuitry will exist on a single piece of silicon. Parallel development of CAN transceivers will also continue through the use of faster and higher voltages process, we should expect to see improvement in the performance of CAN transceivers in the market place.

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