CAN network design and verification using behavioral modeling languages

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Abstract: Prototype level evaluation and verification of communication networks in various configurations over all possible corners, temperature ranges, etc. is a time consuming and expensive task. Moreover only certain corners coming from tolerances of all network parts (cables, common mode chokes, ESD protections) can be evaluated by measurements. Proper behavioral modeling of all network components including relevant corners conditions, allows handy verifications by simulation in early development stages and brings significant improvement in terms of cost and time to market for network designers. Modeling of a full network prior to prototyping can also serve as input for e.g. semiconductor manufactures to develop new transceivers based on simulation results.

The paper deals with behavioral models of CAN bus transceivers. To allow various kinds of verification simulations in a reasonable CPU time starting from basic verifications up to detailed signal integrity analysis, thermal behavior, etc. a set of three behavioral models of a commercial CAN bus transceiver has been developed. The models were developed in VHDL AMS language with accuracy, speed and convergence trade-off being addressed.

A network of CAN transceivers was simulated in various operating conditions and the results prove the effectiveness of chosen approach.

1. Introduction

Controller-Area-Network (CAN) networks complexity is being increasing significantly as application demands in industrial as well as automotive domains do as well [1], [2], [3], [4]. It is estimated that around 400 million CAN nodes were sold in 2005 [1],[2]. The design and verification process of CAN networks is time consuming and expensive as some iteration steps between design and verification are needed. A reliable and efficient methodology must be implemented to effectively manage development risks and verification issues.

The proposed methodology to address previous issues is based on behavioral simulation for assessing verification and fast prototyping of CAN bus networks [5], [6]. Behavioral modeling of all network components, including relevant corners conditions, allows handy verifications by simulation in early development stages and brings significant improvements in terms of cost and time to market for network designers. Behavioral modeling and simulation can tremendously simplify the integration of CAN networks into applications.

In this paper we present a tool (a CAN bus transceiver behavioral model in VHDL– AMS [7],[8],[9]) and a methodology for CAN networks development. The VHDL-AMS language was chosen mainly because it is widely supported for current available mixed-mode circuit simulators. Besides, VHDL-AMS provides features for modeling the digital and analog domains and the communicating interface between them. It is an IEEE open standard [10].

First of all, the paper reports our recent achievements in behavioral modeling of CAN bus transceivers. In particular it introduces a set of three behavioral models of a commercial CAN bus transceiver. The models were developed in VHDL-AMS language with accuracy, speed and convergence trade-off being addressed. CAN bus transceivers and CAN bus

networks are mixed signal systems then behavioral modeling is particularly challenging if accuracy and efficiency must be achieved at the same time. Proper modeling methodology and approach must be implemented.

Secondly the paper introduces related results which aim to demonstrate that:

- the transceiver model is accurate. To this aim, we present a signal integrity analysis by comparing behavioral simulations results with experimental measurements.
- the tool that we propose can effectively simplify the design of the system by significantly decreasing simulation effort and costs if compared with more conventional and less structured approaches like device level simulations using SPICE-like simulators.
- one can validate a CAN network design using behavioral simulation. In this case we introduce behavioral simulation results of a network with line model and with injected faults and compare simulations results with measurements. The simulation results highlight that one can verify (in real operating conditions) the network behavior in a reliable way.

The paper is organized as follows. In Section 2 the state of the art in the field of behavioral mixed mode CAN bus transceiver modeling is reported. Section 3 introduces the CAN bus transceiver VHDL–AMS behavioral modeling methodology and model. Section 4 reports experimental results. Conclusions and future work are drawn in Section 5.

2. Behavioral mixed mode CAN bus transceiver models

To the best of the author's knowledge, there are not mixed-mode behavioral models for CAN transceivers reported in literature. Even where some reference to available models [11] is done, the transceiver model itself is not presented in a formal and systematic way in order to proof his completeness and major performance aspects as computational effort and accuracy. Moreover, many of published works that present tools for CAN networks analysis and validation (see [2],[12],[13],[14],[15]) do not include any aspects related to CAN physical layer. The authors acknowledge the availability of behavioral models for CAN transceivers in current available circuit simulators. However, once again no documentation related to features and/or performance could be found. This work shows an insight of the mixed-mode behavioral model developed for a currently available CAN transceiver: the AMIS-42668 [16]. The results reported in Section 4 are compared with measured data and clearly demonstrate that the proposed model can be effectively used to assess the physical layer behavior of CAN network implementations.

The block diagram of the CAN bus transceiver mixed-mode behavioral model is shown in Figure 1. The analog module converts the I/O signals, represented in the analog domain, to standard logic signals for the digital module. Digital output signals are also converted to analog. It means that all the I/O signals are represented in the analog domain. This feature allows the model to be mixed with device level models within electrical simulation tools (i.e. SPICE-like simulators) that support both kinds of modeling approaches.

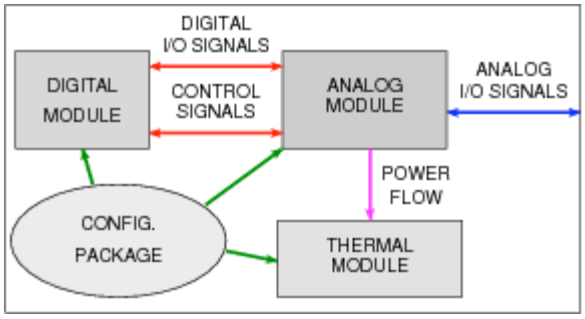

Figure 1 Block diagram

The model is on purpose clearly structured into sub-modules to allow easy customization. This characteristic is useful also for verifications of System Basis Chips (SBC)[1] with integrated transceivers and for the creation of more complex SBCs models.

The analog module is also able to model the instantaneous power consumption based on the actual device operating mode. This feature permits the thermal behavior modeling and the accurate total power consumption estimation. Internal operating

[1] System Based Chips (SBC) are integrated systems that combine several popular functions (i.e. bus drivers, voltage regulators, wake-up switches, SPI, etc.). They are typically used in automotive MCU-based systems.

temperature is computed by the thermal module indicated in Figure 1.

The configuration package allows the user to easily set the transceiver model parameters. It also allows the analysis of the entire CAN system behavior at corner values of the device specifications.

Among others, the following characteristics presented in the transceiver device were implemented:

- CAN bus bitwise arbitration;
- Output voltages slope control to minimize EME;
- Bus short-circuit conditions modeling;
- Maximum output current limiter;
- Voltage references reflect power-supplies states;
- Instantaneous power consumption estimation based on the operating mode;
- Temperature behavioral modeling and thermal shut-down based on the instantaneous power consumption estimation.

3. CAN bus transceiver behavioral modeling methodology

An accurate model is very important for signal integrity assessment. Moreover, simulation speed-up is a mandatory feature of behavioral models. At last but not least, the simulated system complexity needs a special attention on convergence issues. These three issues must be managed, and unfortunately their requirements go to different directions.

The methodology used to face the mixed-mode behavioral modeling requirements, concerning speed and accuracy issues, consists of mixing different modeling abstractions levels and mathematical approximations in order to model each single block behavior within the transceiver structure. Piecewise linear, exponential functions and Taylor series approximations were used. Different performance in terms of accuracy, speed and convergence were noticed. Moreover, some transceiver functions were described using high level statements while others making use of hierarchical description using a low level abstraction modeling approach where used devices description is as close as possible to its real operation. As a consequence, a set of basic building blocks has been implemented. The methodology modularity was exploited according to Table 1. More details about the methodology and building blocks construction can be found in [5] and [6].

Table 1 shows three different implemented architectures. Different approximations and features were arranged in each architecture: the user can arbitrarily choose one of them according to the accuracy level and simulation speed required for a given analysis. Nonetheless, a minimum set of features is present in all architectures allowing meaningful basic signal integrity and/or devices behavior analysis for any combination of the model architectures inserted in a CAN bus system simulation.

4. Experimental results

In this section, we present some results to illustrate the model performance. Simulation results are compared with experimental measurements. The setup used for both simulations and measurements is illustrated in Figure 2. Please note that, due two the difficulty of precisely take into account the transmission lines and power supply lines effects, a simple setup has been used. Nonetheless, a simple setup in first step model evaluation allows fast feedback and easier analysis and understanding of first order effects.

Two transceivers nodes were connected to the bus with 0.5 m long cables. Termination of the bus was modeled including small inductance (50.0nH) and scope probes capacitances (10.0pF) used during

	Fast	**Moderate**	**Accurate**
Output Drivers	Piecewise linear	Taylor series	Transconductor
EME control	NO	NO	YES
Internal Voltage Reference	Piecewise linear	Exponential	Exponential
Power Consumption Estimation	NO	YES	YES
Thermal Shutdown	NO	YES	YES

Table 1: CAN transceivers model architectures characteristics

measurements. For all bus short-circuits cases the inductance of the shorts was modeled.

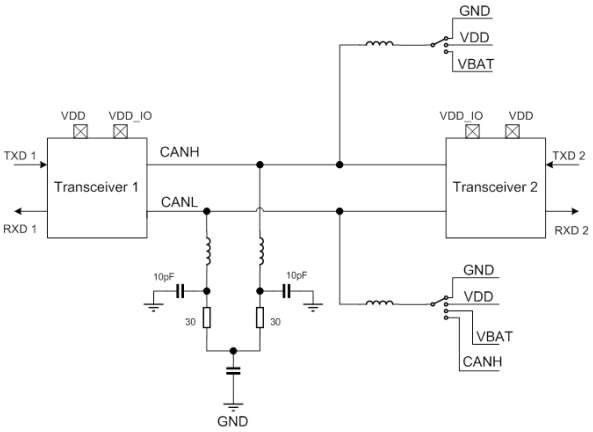

Figure 2 - Test-bench setup

Results are organized as follows. In the first set, we assess signal integrity of behavioral model simulation results by comparing them with measurements.

In the second set, we show the behavioral model performance in terms of CPU simulation effort.

Finally, in the third set we compare behavioral simulation results with measurements of CAN bus network real operating conditions and also in the presence of some disturbances as short-circuits and un-powered nodes connected to the bus line.

4.1 Signal integrity assessment

Figure 3 to Figure 5 show a comparison of measured waves with results using all three VHLD-AMS models architectures. In this case, transceiver power supplies have typical values and no bus error has been injected.

The measured and VHDL-AMS ACCURATE model data match, mainly regarding the bus signals voltage slope. The FAST and MODERATE VHDL-AMS models results still match on voltage levels with measurements during recessive and dominant states. Basic timing delay characteristics are preserved as well. However, one of the important aspects of an accurate representation of such signal variations is that matched CANH and CANL signals determine the involved amount of electromagnetic emission (EME). Symmetrical CANH and CANL signals cause constant common mode voltage and zero common mode current, resulting in no EME. Therefore, considering that FAST and MODERATE model inaccurately signals transitions, these models as such are not suitable for signal integrity, electromagnetic emission (EME) investigations.

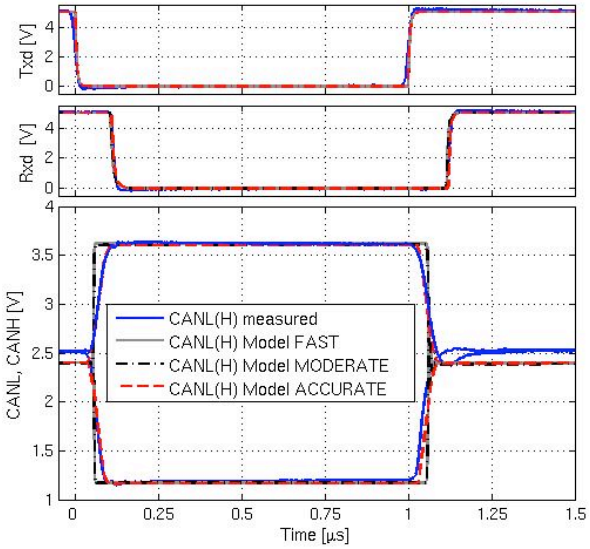

Figure 3 - Successful communication

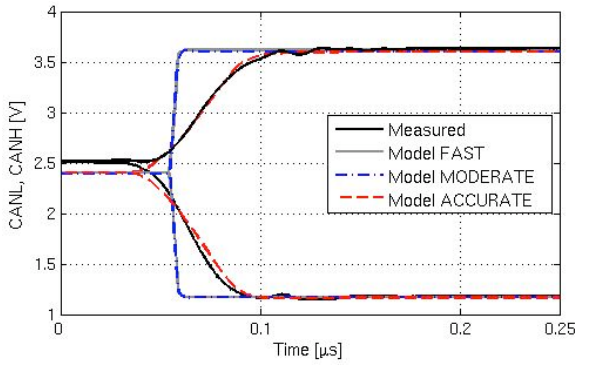

Figure 4 – Recessive to dominant states transition detail

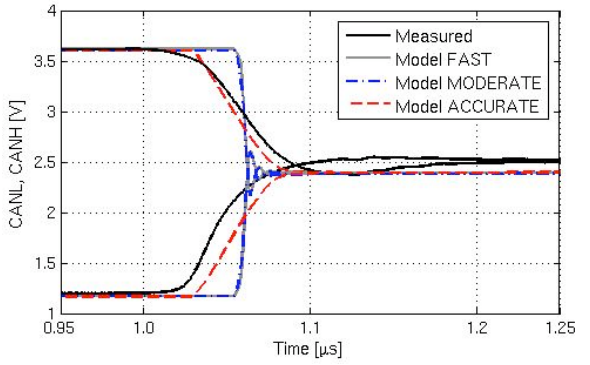

Figure 5 – Dominant to recessive states transition detail

In terms of CPU simulation speed, SPECTRE simulation, despite using behavioral description of computationally expensive parts (e.g. oscillator), was approximated 600 times slower than the

VHDL-AMS ACCURATE model results. Behavioral model simulations also create significantly smaller results database which allows easier systems debugging and results visualization.

4.2 CAN network CPU simulation effort

The three model architectures presented in Table 1 have been tested in several normal and faulty conditions. Table 2 gives a brief description of the main tests. Test cases are of primary importance for the complete model validation. They are useful to verify the analog interface behavior and the information transfer between analog and digital modules as well.
The third column of Table 2 reports the simulation time period for the transient analyses. Table 3 shows the CPU execution time in seconds for each test. The results show that the proposed approach can be used to effectively manage the speed and accuracy trade-off.

TEST #	Description	Simulation Period
Test 1	TXD dominant clamp timeout	1.1ms
Test 2	VIO under-voltage timeout	12.3ms
Test 3	Loop delay TXD-CANBus - RXD	14.us
Test 4	Hoping states	133.1us
Test 5	Short-circuits	210.1us
Test 6	Local and remote wake-up	670.1us
Test 7	Power-On Detection	10.5ms

Table 2: Test cases description

	Fast	Moderate	Accurate
Test 1	46.9 s	49.7 s	59.3 s
Test 2	392.4 s	450 s	534.7s
Test 3	15.2 s	24.2 s	31.3 s
Test 4	18.8 s	28.3 s	35.0 s
Test 5	30.4 s	52.4 s	90.5 s
Test 6	31.8 s	38.0 s	46.5 s
Test 7	339.1 s	390 s	461.0 s

Table 3: CPU usage time

During verifications of more complex transceivers in various operating states (e.g. standby, listen only, sleep, etc.) and mainly when SBCs are included in the network, usage of the fast model is very handy for validation of correctness of all modes transitions, etc.

The usage of the proposed methodology also helps in the functional definition and verification of application specific circuits with integrated bus transceivers in early product stage development helping first time right silicon design success.

4.3 CAN network simulation and verification

In order to demonstrate model accuracy performance, the transient responses in some critical situations are shown in next sections. We applied some fault conditions as, for example, bus lines to power supplies shorts, bus lines to ground shorts, shorts between both bus lines and removal of power supply from one of the network nodes.

The model capability of accurately modeling faults is very useful during CAN systems early development stages. An important consequence is that the time effort and the network prototype costs can be meaningfully reduced.

An interesting feature included in the behavioral model is that it is able to give info and warning messages describing the device operating condition and error messages whenever any absolute maximum ratings of the transceiver is exceeded. This feature has an important and direct impact on the network reliability assessment.

Here, only the ACCURATE model results are compared with measured data because the accuracy of signals representation is of great value. The results obtained for the other two models follow, in general, the dynamic response characteristics seen in Figure 3. In other words, very fast voltages variations that in the presence of the line and shorts-circuits inductances result in overestimated over-shootings. Nonetheless, FAST and MODERTAE models may still be efficiently used when less complex situations must be analyzed.

4.3.1 CAN bus short-circuit fault analysis

Short of CANL bus wire to battery voltage is expected to create zero differential voltage and thus no communication on the bus. Although the value of the resistance modeling the short was virtually equal to zero ohm, due to the inductance of the wire short, pulses in the range of tens nanoseconds and 2.0 V of magnitude are still visible both in simulation and measured data (See Figure 6). Please note the behavioral model is accurate enough to represent the small glitching seen in the RxD signal (due to the different pulse amplitudes of CANH and CANL signals, the differential voltage reaches the threshold level that defines dominant state).

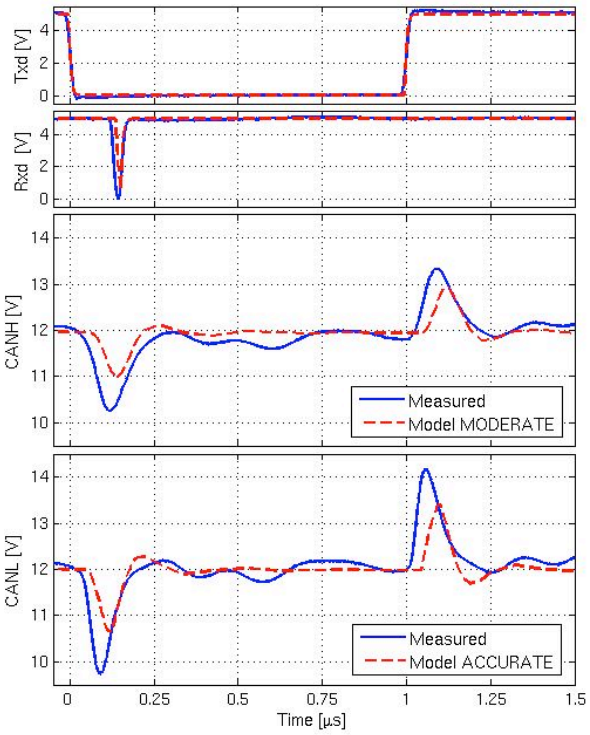

Figure 6 - CANL to battery short-circuit

Figure 7 shows the transient response of a short-circuit between the CANH wire to V_{DD}. This is a case of non destructive communication fault. Power consumption increases as CANL pin driver can pull the bus up to current limitation.

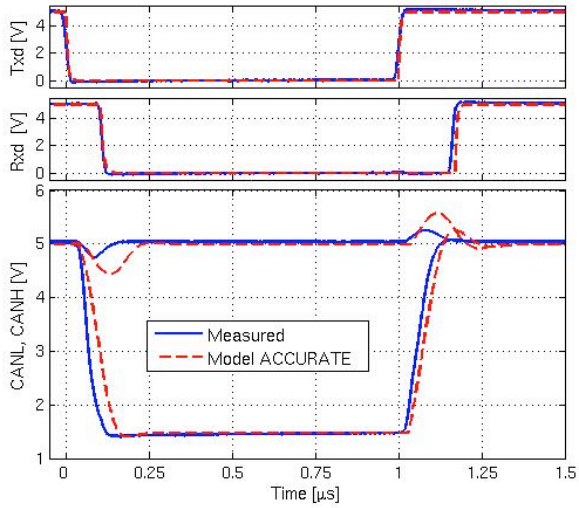

Figure 7 - CANH to V_{DD} short-circuit

As it can be seen in Figure 7, the common mode voltage in recessive states is V_{DD}. When the transceiver tries to send a dominant state, the CANL voltage drops down to about 1.5V as expected during such state. As a consequence, for each dominant to recessive transition the common mode voltage will have a step of around 1.75V which will cause EME being significantly increased mainly in the frequency range of communication. Therefore, even if the communication is possible, the EME performance is compromised.

Figure 8 shows a low ohmic short-circuit condition (much lower than bus line termination resistances) between both CAN bus lines. The resulting common mode voltage in dominant state is strongly dependent on the mismatch between maximum current values of CANH and CANL drivers. Once more the VHDL-AMS model is able to efficiently represent the signals behavior during this fault condition. Consequently, the resulting EME due to common mode voltage variations can be correctly estimated

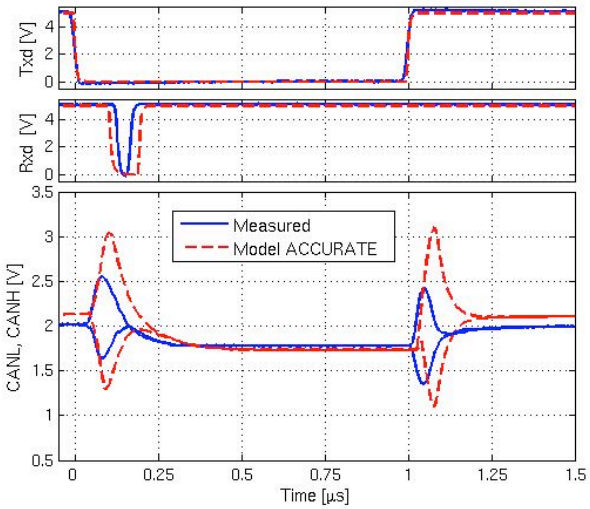

Figure 8 - CANL to CANH wires short

4.3.2 – CAN bus line disturbance caused by a node with power supply failure

A possible network fault situation is the one where one or more transceivers are not powered. In the following case, the transceiver has a power-supply under-voltage detection. It means that if one of the voltages at supply pins drops below a given value, the transceiver is forced into low-power mode. When it enters into such state, it acts as an undesirable load on the bus and it pulls the bus to ground. Instead, in normal mode the transceiver keeps bus wire voltage biased around midway the supply voltage range. The fault again results into non optimal EME performance while communication in terms of differential voltage value is not affected.

The case presented here represents a worst case condition as it shows two nodes one of which is not powered. In larger size networks influence of not power supplied transceivers is minimized by impedance of power supplied transceivers.

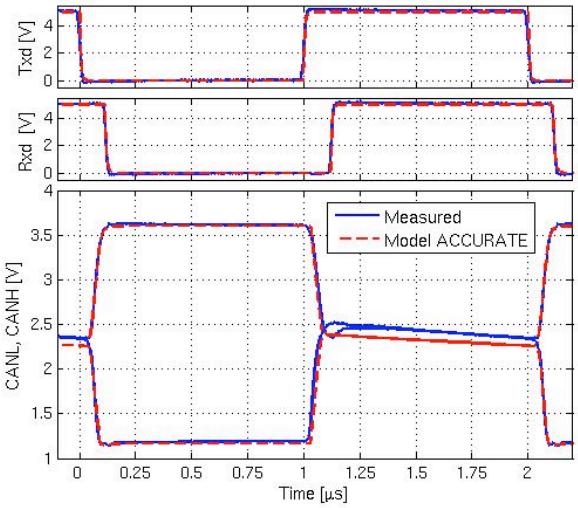

Figure 9 - Un-powered node influence to communication at 1MBaud/s

Figure 10 shows a situation when lower speed of communication (very often used in industrial applications) is used and an unpowered node is present. The result is that the unpowered node strongly pulls the network to ground during recessive state.

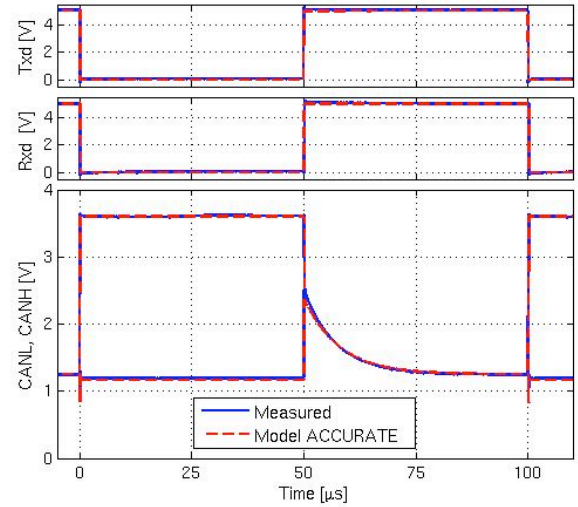

Figure 10 - Un-powered node influence to communication at 20KBaud/s

4.3.3 Power consumption and thermal behavior

The VHDL-AMS model includes power consumption estimation and thermal behavioral modules. Figure 11 shows a case where the model estimates the power consumption considering both bias and output currents, and models the junction temperature variation based on the power consumption.

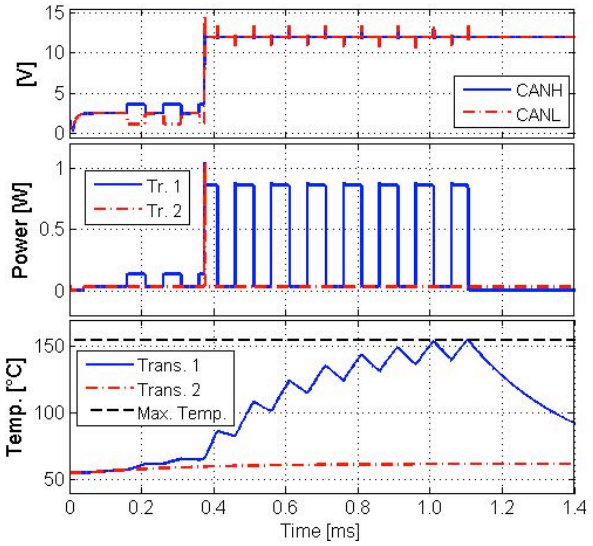

Figure 11 - Power consumption and thermal behavior during short-circuit

In this example, the transceiver "1" tries to send a stream of recessive and dominant states while a short-circuit of CANL node to battery is present. This short represents the worst situation for transceivers from the power dissipation point of view. The device temperature increases gradually. When the temperature limit is reached, an over-temperature signal is generated (not shown for simplicity). Then, the transceiver "1" disables its output driver. Doing so, the excessive power dissipation vanishes and the temperature drops down, saving the device from a destructive damage. Instead, for the transceiver "2", that it is not trying to access the bus, only the bias power is consumed and the power dissipation is lower. Therefore, its temperature remains much lower than that of transceiver “1”.

5. Conclusions and future work

The presented modeling methodology allows to check functional behavior and signal integrity of the CAN bus networks in a cost efficient way. The model proved to be able to accurately model many electrical aspects of CAN bus transceivers; a special attention was given to fault conditions analysis

The possibility to validate the network in corner situations, as well as with other network elements (e.g. terminations, common mode chokes, cables, etc.) and reliability related aspects (e.g. operating

range check, absolute maximum ratings violation, and thermal behavior) gives to network designers a tool for more efficient design development.

When more precise models of CAN bus components will be available, the model features, mainly in terms of signal integrity and fault condition modeling, will be further analyzed. Model parameters based on fine tuning on direct comparisons between simulation and measurement results are currently being carried on.

The great level of modularity used to develop the models allows an easy customization of internal blocks. Therefore, a wide range of devices can be modeled using the presented methodology. Models for two transceivers, AMIS42668 and AMIS42665, are currently available. We plan also to develop behavioral models of Flexray transceivers (10Mbit/s) and some others SBC devices.

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