Bit Time Requirements for CAN FD

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The new CAN FD frame format that is currently being integrated into ISO 11898-1 introduces a second bit time configuration into CAN networks. While the nominal CAN bit time is still used at the beginning and at the end of the frames, for arbitration and for acknowledge, called the Arbitration Phase; the new data bit time may be used for the main part of the frames, called the Data Phase. The data bit time may be shorter than the nominal bit time in order to speed up frame transmission.
This paper describes the constraints for the CAN FD bit time configuration and how to harmonize the two bit rates for smooth switching between them. It also describes the transceiver delay compensation mechanism which is needed for data bit times that are in the range of or even shorter than the transceiver loop delay.

Introduction

In April 2012, Version 1.0 of the CAN FD Protocol Specification [1] was released, introducing the CAN FD Frame Format (see 0) into the CAN protocol. This new format allows more than 8 data bytes in one frame and gives the option to transmit the central part of the frame at a higher bit rate than in classical CAN communication.
The first implementations of the CAN FD protocol were available as IP modules [2] for laboratory evaluation. Meanwhile CAN FD is also available in silicon, as module on μCs from ST (SPC57EM80) or from Freescale (Qorivva MPC5748G). CAN network tools are also upgraded to CAN FD, e.g. by Vector and by ETAS.
Higher layer protocols (e.g. CANopen, CAN4Linux, SocketCAN, ISO 15765-2, J1939) are adapted for CAN FD, and the new frame format is currently being integrated into ISO 11898-1 [3], the main CAN standard document.
NXP have released the first transceivers (TJA1044GT, TJA1057GT) for CAN FD communication, they fulfill the automotive OEMs' EMC requirements at bit rates up to 2 Mbps.

CAN FD Frame Format

ISO 11898-1 is currently being expanded to include the CAN FD Frame Format. The existing frame formats are not changed, they are now named "Classical Frame Formats". There have been editorial changes when the FD Frame Format was introduced into ISO 11898-1. Differing from [1], the bit EDL is now named FDF (**FD F**ormat) and the two dominant reserved bits r1 and r0 are now named RRS (at the position of the classical RTR bit) and res (after the FDF bit). Their function is the same as before.

CAN FD Standardization

The "FD Frame Format" supplements the CAN communication; it does not substitute the existing "Classical Frame Format". Existing CAN implementations will be able to coexist with new implementations in the same network if only Classical Frames are used or if they are not active while frames in FD Format are transmitted. In future, there will be three types of CAN implementations: "FD enabled" which can send

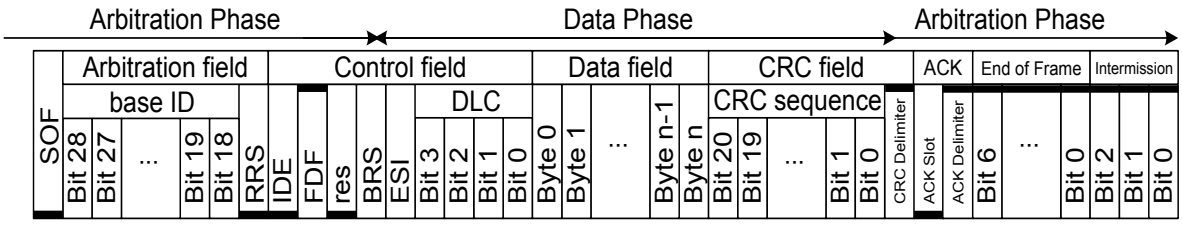

Figure 1: CAN FD Frame with 11 bit identifier and with more than 16 Data Bytes

and receive the “FD Frames”, “FD tolerant”, which do not disturb the “FD Frames”, and the legacy CAN implementations, which only understand the “Classical Frame Format”. Standardized CAN Conformance testing according to ISO 16845 will be possible for each of the three types.

Bit Rates in the FD Frame Format

The FD Format was introduced to increase CAN’s net throughput. That is achieved by two new features of the FD Format. The first is the extended range of the data field which allows up to 64 data bytes in one frame, improving the frame’s header/payload ratio and reducing the need for transport protocol frames. The second is the option to transmit part of the frame, the Data Phase, at a higher bit rate than the nominal bit rate of the CAN communication. The higher bit rate is called the data bit rate and uses the data bit time.
CAN nodes synchronize on observed edges on the CAN bus, but the signal propagation time on the bus line introduces phase shifts between the nodes. CAN’s non-destructive arbitration mechanism for media access control requires that the phase shift between any two nodes is less than half of one bit time, see also [5]. This lower boundary for the nominal bit time defines an upper boundary for the nominal bit rate as well as for the bus length.
The configuration of the nominal CAN bit time, especially the Propagation Segment’s length and the Sample-Point’s position, must ensure that twice the maximum signal propagation time fits between the Synchronization Segment and the Sample-Point. The FD Frame format uses the same arbitration mechanism and therefore must conform to the same configuration rules for the nominal bit time.
The signal propagation time between the nodes needs to be considered when more than one node may transmit a dominant bit. This is the case in the arbitration field or in the acknowledge slot. Once the arbitration is decided, until the end of the CRC Field, only one node transmits dominant bits, all other nodes synchronize themselves to this single transmitter.
Therefore it is possible to switch to a predefined (shorter) bit time in this part of an FD CAN frame, the Data Phase. The Data Phase starts in the frame’s control field and ends at its CRC delimiter, see 0. The rest of the CAN communication, outside the Data Phase, is called the Arbitration Phase. The data bit rate is used during the Data Phase; CAN’s nominal bit rate is used outside the Data Phase.

Switching the Bit Rates in the FD Frame

CAN nodes synchronize on received edges from recessive to dominant seen on the CAN bus line. The aim is to maintain the distance between the edge and the Sample-Point. Edges are expected to be seen in the Synchronization Segment. If a received edge is seen between the Sample-Point and the Synchronization Segment, it is considered an early edge (with a negative phase error) and the Phase Buffer Segment 2 is shortened. If a received edge is seen between the Synchronization Segment and the Sample-Point, it is considered a late edge (with a positive phase error) and the Phase Buffer Segment 1 is lengthened. All nodes will see their own transmitted edges to be late, caused by the transceiver loop delay. Therefore a node sending a dominant bit does not synchronize on late edges, otherwise that bit would be lengthened by the amount of the loop delay.
The phases of the receivers’ Sample-Points are shifted relative to the phase of the transmitter’s Sample-Point. A node’s specific phase shift has a static component, caused by the signal propagation time from the transmitter to that specific node and a dynamic component, caused by the difference in clock speed between the two nodes. The maximum time between two edges used for synchronization is 10 bits, guaranteed by CAN’s bit stuffing mechanism. The dynamic phase shift caused by a clock tolerance of 1% may accumulate to 20% of a bit time before the next synchronization.
Once a receiver is synchronized to a transmitter, e.g. by hard-synchronization at SOF, the static phase shift will not cause further phase errors. The formulas for the

CAN clock tolerance ensure that the dynamic phase shift between transmitter and receiver remains at a lower value than the SJW, the (re-)synchronization jump width, which is the maximum phase error that can be corrected by one synchronization.
The dynamic phase shift must be minimized before switching from the nominal bit time to the shorter data bit time, it may not exceed the SJW of the data bit time.
This is one of the reasons why the FD Frame Format separates between detecting the format at the FDF bit and switching the bit rate at the BRS bit. The other reason is that it gives the option to transmit a frame in FD format but only using the nominal bit rate. This can even be used as a fallback option when the physical layer is degraded by external disturbances.
There may be several transmitters during arbitration, and transmitters do not synchronize on late edges, so a node that loses arbitration at the last bits before the FDF bit may not yet be synchronized to the remaining transmitter. This node will synchronize at the edge from the FDF bit to the res bit. To ensure that the phase error is corrected completely, regardless of the size of the SJW, the synchronization at that edge is a hard-synchronization.
An example for bit rate switching is shown in Figure 2. This figure shows a simulation in the testbench of the VHDL CAN Reference Model. The two nodes RefCAN1 (transmitting an FD Extended Frame) and RefCAN2 (transmitting a Remote Extended Frame with the same identifier) arbitrate for bus access. RefCAN2 loses arbitration when it transmits the recessive RTR bit and samples (see ①) RefCAN1's dominant RRS bit.
RefCAN2 samples the recessive FDF bit, recognizes the FD Format, and enables the hard-synchronization. Before that, RefCAN1's Sample-Point comes before RefCAN2's Sample-Point; after the hard-synchronization, it comes after that of RefCAN1. The phase shift shown at ② is the signal propagation time between the nodes. Both nodes switch to the (in this example much) shorter data bit rate at the Sample-Point of the recessive BRS bit shown at ③.

Note that in this example the static phase shift between the two nodes is larger than one data bit time.

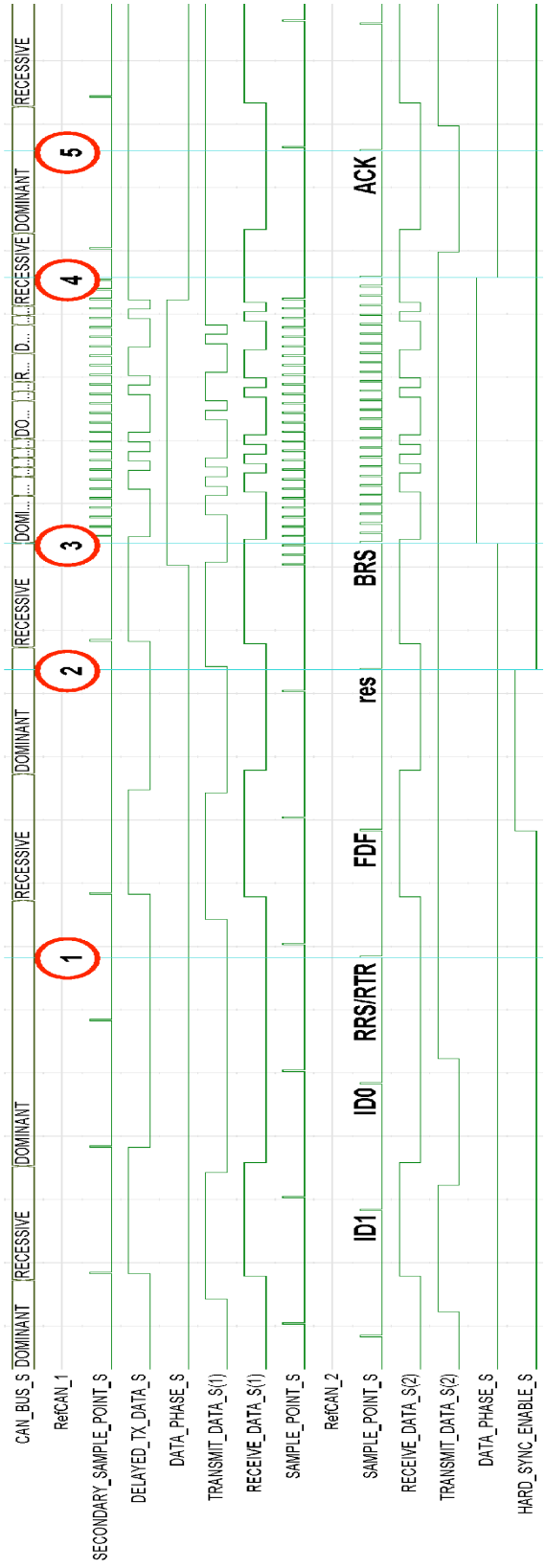

Figure 2: Data Rates in an FD Frame

The nodes switch back to the nominal bit time at the CRC Delimiter, ④. No hard-synchronization is necessary at this bit rate switch, since the possible residual dynamic phase shift can be compensated by the following larger SJW, see also [6]. The transmitter synchronizes on the edge to the dominant ACK bit at ⑤, reversing the static phase shift between the nodes.

Configuring the Nominal Bit Time

The nominal bit time is configured according to the conditions described in [5], with one additional requirement. Since the bit synchronization mechanism operates with a time resolution of one time quantum, a phase error of up to one time quantum may remain after synchronization. When switching from the Arbitration Phase to the Data Phase, the current phase error is passed on. For optimum performance, the length of the nominal time quantum should therefore be no longer than the data time quantum. Also, the Sample-Point must be configured to the same position in all nodes of the network. Having the same number of time quanta in the nominal bit time and in the data bit time and switching the bit rate just by changing the length of the time quantum via the baud rate prescaler will not work in most cases.
The whole set of formulas to calculate the optimum bit time configurations regarding oscillator tolerance, transceiver asymmetries, bus length, and physical layer topology are given in [6].
Since short data time quanta are needed to enable a short data bit time, and the same time quantum should be used in the nominal bit time, the number of time quanta in a nominal bit time needs to be increased in a CAN FD network compared to a classical CAN network.
The first implementations of the CAN FD protocol (see [2]) have increased the configuration range of the nominal bit time's Propagation Segment up to 48 time quanta and the range of the Phase Buffer Segments as well as the SJW up to 16 time quanta.

Configuring the Data Bit Time

The data bit time consists, like the nominal bit time, of four segments: Synchronization Segment, Propagation Segment, and the two Phase Buffer Segments. Each segment consists of an integer number of data time quanta. Receivers follow the same synchronization in the Data Phase as in the Arbitration Phase while transmitters do not synchronize at all in the Data Phase.
Since the static phase shift between transmitter and receiver is not relevant in the Data Phase, the Propagation Segment may be set to a length of 0 time quanta. This allows making the Buffer Segments and the SJW larger, giving more freedom in placing the Sample-Point. The Sample-Points should be placed in the middle between the time when the bus signal has stabilized after a possible late edge at the beginning of the bit and a possible early edge at the end of that bit.
The example shown in Figure 2 operates with an 80 MHz system clock, resulting in a time quantum length of 12.5 ns. The length of the nominal bit time is 1000 ns, or 80 time quanta (1+47+16+16). The nominal bit rate is 1 MBit/s. The data bit time in that example is 75 ns, or 6 time quanta (1+0+3+2). The data bit rate is 13.33 MBit/s. While the nominal bit time in the example is realistic, the data bit time is not. The short data bit time was chosen, together with a DLC of 0, in order to be able to show the complete Data Phase of an FD Frame in one figure.

Configuration Example

A realistic bit time configuration example is given in Table 1 based on a system clock of 20 MHz. This configuration can be used with CAN transceivers that are newly released for CAN FD bit rates up to 2 MBit/s.

Table 1: CAN FD Bit Configuration

Bit Time Parameter	Nominal	Data
System Clock	20 MHz	
Time Quantum (tq)	50 ns	50 ns
Sync_Seg	1 tq	1 tq
Prop_Seg	23 tq	1 tq
Phase_Seg1	8 tq	4 tq
Phase_Seg2	8 tq	4 tq
Bit Length	40 tq = 2 μs	10 tq = 0.5 μs
Bit Rate	0.5 MBit/s	2.0 MBit/s
SJW	8 tq	4 tq

Nominal and data bit time both use the minimum time quantum of 50 ns (BRP=1).

The nominal bit time makes use of the extended configuration range for the bit segments. It uses 40 tq to generate the 2 μs long bit time needed for the bit rate of 0.5 MBit/s that is used in most automotive applications.
The data bit time places its Sample-Point more to the middle of the bit, not needing to compensate for signal propagation time.

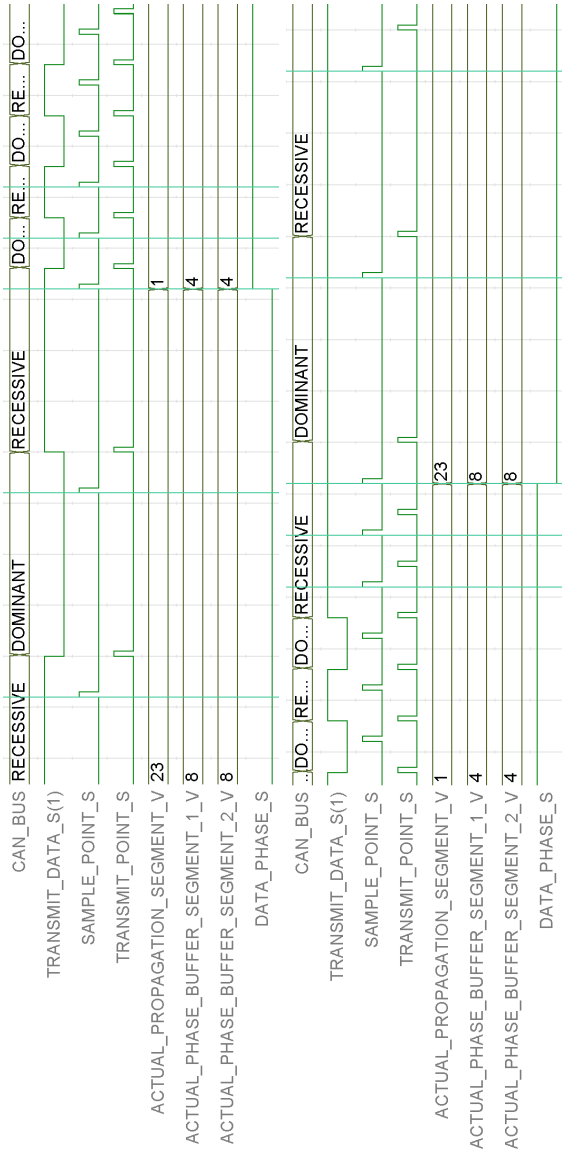

Figure 3: Start and End of Data-Phase

Figure 3 shows how the CAN FD controller switches automatically between the two sets of bit time configuration parameters, at the start of the Data Phase (Sample-Point of the BRS bit) and at its end (Sample-Point of the CRC delimiter). Although the bits BRS and CRC delimiter are of intermediate length (different bit time parameters before and after the Sample-Point), note that the distance between the Sample-Points is always one nominal bit time or one data bit time, when not synchronizing to an edge on the CAN bus.

Transceiver Delay Compensation

All transmitters check, at the Sample-Point, whether the previously transmitted bit is sampled correctly. Apart from arbitration, this mechanism is needed to check for problems in the physical layer and to detect other node's error frames. Since the transmitter sees its own transmitted bits delayed by the transceiver loop delay, this delay would set a lower limit to the length of the data bit time, which also would be an upper limit to the data bit rate.
This is the reason why the Transceiver Delay Compensation mechanism (TDC) was introduced.
In order to compensate for this loop delay when checking for bit errors, a Secondary-Sample-Point (SSP) is defined. Instead at the Sample-Point, the transmitted bits are checked at the SSP. The result of that check is stored until the next Sample-Point is reached, where the protocol controller FSM is evaluated. Only transmitters need the TDC mechanism, since receivers do not drive any bits during the Data Phase.
An SSP is generated for each bit transmitted in the Data Phase. The position of the SSP needs to be placed in the middle of the time interval that starts when the bus signal has stabilized after a possible edge at the beginning of the bit and ends before a possible edge at the end of that bit. Transceiver asymmetry and ringing on the bus have to be considered for the SSP position, but no clock tolerance, since the transceiver monitors its own bit stream.
The transceiver loop delay must be known, either from the transceiver's data sheet, or from a measurement. Figure 4 shows how the actual loop delay is measured inside an FD Frame, before the beginning of the Data-Phase. A counter is started when the transmitter starts to drive its CAN_Tx pin with the dominant res bit after the FDF bit. The counter is stopped when the dominant level is seen at the CAN_Rx pin. The counter value is the measured loop delay (unit: clock periods).

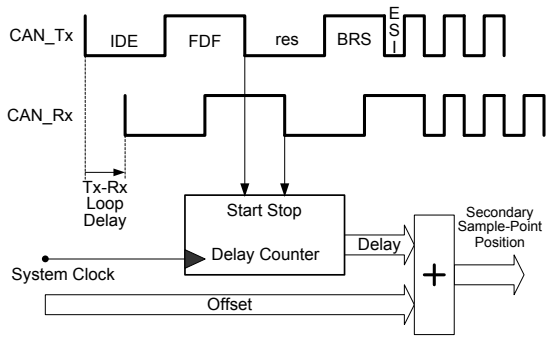

Figure 4: Loop Delay Measurement

The SSP position is given relative to the start of the transmitted bit, it is either configured to a constant value or it is the sum of the measured loop delay plus a configured offset.

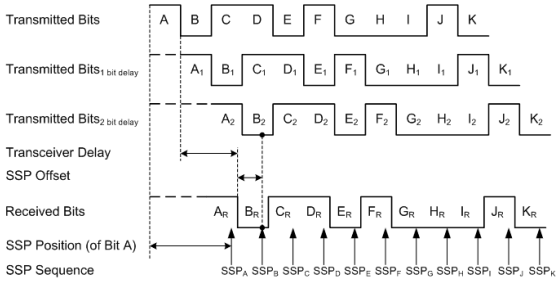

Figure 5: Trv. Delay Compensation

The value of a transmitted bit is stored until its SSP is reached, then it is compared with the actually received bit value, as shown in Figure 5. Here a transmitted bit sequence A...K and a received bit sequence A_R...K_R is shown, together with a sequence of SSPs from SSP_A to SSP_K. The received bit B_R is checked at SSP_B by comparing it with the delayed bit B_2. The position of SSP_B is at a specific time after the start of the transmitted bit B. This specific time is the sum of the measured transceiver delay and the configured SSP offset. The TDC mechanism, with delayed transmitted bits and SSPs, is also demonstrated by the simulation example in Figure 2.

No TDC is needed for data bit rates up to 2.5 MBit/s; here the maximum loop delay is elapsed before reaching the regular Sample-Point.

Conclusion

The same restrictions that limit the bit rate in classical CAN communication are still valid for the nominal bit time of CAN FD communication, required for the CAN bit arbitration and acknowledge mechanisms. These two mechanisms are not used in the FD frame's data phase; they therefore do not constrain the data bit time configuration. The data bit time needs to be coordinated with the nominal bit time in order to optimize the transition from one bit rate to the other.

The minimum length of the data bit time depends on the properties of the CAN physical layer. A transceiver delay compensation mechanism is introduced to make the length of the data bit time independent from signal propagation time.

Standardization of CAN FD is in progress, it is introduced into ISO 11898-1; and into ISO 16845 for conformance testing.

First silicon is available, both for protocol controllers and for transceivers, which allow setting up CAN FD networks with a bit rate of up to 2 MBit/s in automotive applications.

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