The physical layer in the CAN FD world
The update

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In automotive and industrial applications the CAN protocol is very well established. But in this applications more and more data will be used and the limitation of the classical CAN network with 1 Mbit/s was not sufficient for the future. With bit rates up to 5Mbit/s, the improvement of CAN called CAN FD is now available to increase the average data rate. An update of the physical layer requirements for this high bit rates was necessary and all new and modified parameters are described in this article.

For CAN physical layer the ISO specifications 11898-2/5/6 are relevant. These three specifications are now merged into one specification ISO11898-2 (ed. 2016), which will be released beginning of 2016. In these updated specification additional dynamic parameters for CAN FD and higher bit rates are added and a lot of existing parameters are modified and adjusted for future needs. The dynamic parameters, relevant for CAN FD will be discussed first.

General

During arbitration phase, when two or more nodes are in competition to win the arbitration, the max bit rate is limited by

- Network propagation delays
- Transceiver propagation delays
- And reflection.

After the arbitration phase, the propagation delay between nodes is not important anymore but the bit width variations, caused by the network behavior and the transceiver performance, are relevant. What are the reasons for bit width variations? Which parts of the network determine the bit width variation?

- The interface between micro-controller and transceiver
- The transceiver
- The network (reflection, damping)

The transceiver has three different propagation delays

- Loop delay TxD to RxD
- Transceiver Tx (Transmitter) delay
- Transceiver Rx (Receiver) delay.

The symmetry requirements of these delays are now added in the ISO 11898-2 and will be described in the next chapters.

Loop delay symmetry

The loop delay is the delay between the TxD input signal and the RxD output signal of a transmitting transceiver.

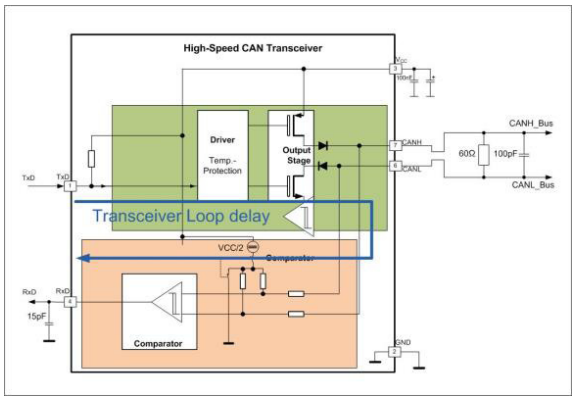

Figure 1: Transceiver Loop delay symmetry test circuitry

Figure 1 illustrates the loop delay. The trigger level for the recessive to dominant edge is specified to 30 % and for the dominant to recessive edge to 70 %. Figure 2 shows, how the loop delay is specified. The symmetry of these both delays is very important for the transmitting node and may be different.

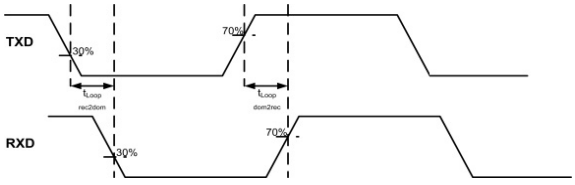

Figure 2: Transceiver Loop delay specification

To check this dynamic performance the recessive bit-time on the RXD pin ($t_{Bit(RXD)}$) after five consecutive dominant bits is defined (see Figure 3). If the transceiver is very asymmetric, the recessive bit-time will be shortened or expand compared to the nominal bit time.

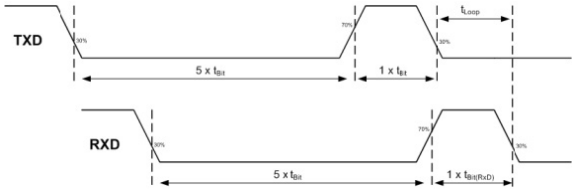

Figure 3: Transceiver loop delay symmetry specification

In Table 1 the specified characteristics are shown. In Figure 4 the impact on a RxD signal is demonstrated. The recessive signal has a wide range of variation and the sample point should be set as late as possible. The max propagation delay TxD to RxD for both edges is below 255ns.

Table 1: Loop delay symmetry characteristics

Bit rate (data-phase)	Recessive $t_{Bit(RXD)}$ min	Recessive $t_{Bit(RXD)}$ max	t_{bit} nominal	Load on CAN Bus
1 Mbit/s	n.a.	n.a.	1000 ns	60 Ωll100 pF
2 Mbit/s	400 ns	550 ns	500 ns	60 Ωll100 pF
5 Mbit/s	120 ns	220 ns	200 ns	60 Ωll100 pF

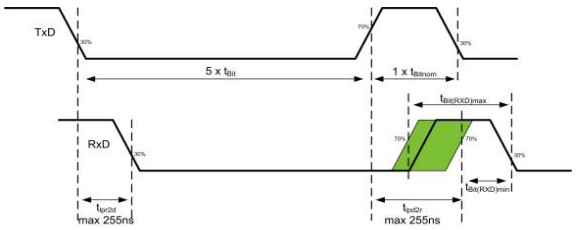

Figure 4: Transceiver Tx delay symmetry

In general, an asymmetric behavior is caused by

- the busload (resistive and capacitive)
- the maximum differential voltage of the dominant bit
- the temperature dependency of the transceiver internal delays.

Transceiver Tx delay symmetry

The Transceiver Tx delay is the delay between the TxD input signal and the differential bus output signal. The symmetry is the difference between the recessive to dominant delay and the dominant to recessive delay.

The recessive to dominant propagation delay is specified from 30 % of the TxD signal to 900mV of the bus differential voltage. The dominant to recessive propagation delay is specified from 70% of the TxD signal to 500mV of the bus differential signal. Both propagation delays should be equal but they may be different.

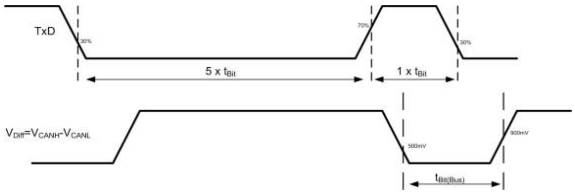

Figure 5: Transceiver Tx delay symmetry

One reason for the asymmetry is the internal delay from TxD Pin to the output stages. The second reason is the differential level of the dominant signal. This dominant level depends on

- Transmitter supply voltage
- Physical bus load
- Transceiver temperature

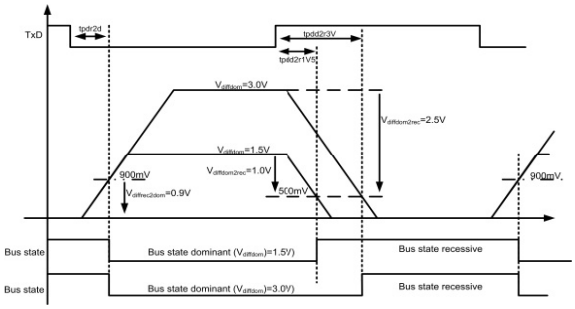

Figure 6: Dependency of Vdiff dominant voltage level and propagation delay symmetry

To reduce the emission of transmitting signals, the slew rates are controlled and as slow as possible for high bit rate. The voltage difference between the recessive level and the dominant threshold level are always 900 mV (see Figure 6).The slew rate is fix and defines the delay time. The difference between dominant level and the recessive threshold can differ from 1 V (1.5 V dominant level minus 500 mV recessive threshold) up to 2.5 V (3 V dominant level minus 500 mV recessive threshold). Due to the fixed slew rate, the dominant to recessive delay time depends on the level of the dominant signal. In Figure 6 two scenarios illustrated with the lowest possible and highest possible dominant voltage level. In this scenario the

impact of the bus load is ignored. In Table 2 the new parameters for the transmitter are illustrated.

Table 2: Transceiver Tx delay symmetry characteristics

Bit rate (data-phase)	$t_{Bit(Bus)}$ min	$t_{Bit(Bus)}$ max	t_{bit} (nominal)	Load on CAN
1 Mbit/s	n.a.	n.a.	1000 ns	60 ΩII100 pF
2 Mbit/s	435 ns	530 ns	500 ns	60 ΩII100 pF
5 Mbit/s	155 ns	210 ns	200 ns	60 ΩII100 pF

Transceiver Rx delay symmetry

The Transceiver Rx delay is the propagation delay between the differential bus input signal and the RxD output signal. This symmetry depends on

- Production dispersion
- Temperature variation
- The Receiver thresholds
- Supply voltage variation
- Bus differential voltage Vdiff slew rate

Δt_{Rec} is a calculated value. The calculation formula is:

$$\Delta t_{Rec} = t_{Bit(RxD)} - t_{Bit(Bus)}$$

Table 3 shows the defined values. $\Delta t_{Rec\ (min)}$ shortens the recessive bit length and $\Delta t_{Rec\ (max)}$ expands the recessive bit length.

Table 3: Transceiver Rx delay symmetry

Bit rate (data-phase)	Δt_{Rec} (min)	Δt_{Rec} (max)	t_{bit} (nominal)
1 Mbit/s	n.a.	n.a.	1000 ns
2 Mbit/s	-65 ns	40 ns	500 ns
5 Mbit/s	-45 ns	15 ns	200 ns

Bit timing symmetry in a network

Figure 7 illustrates the Link between

- TxD signal on the transmitting node
- Bus differential voltage Vdiff and its variation
- The possible recessive bit-time duration at the receiving node's RxD pin.

The rising edges may jitter. The falling edges are stable, as this is the edge on which a CAN node synchronizes and this dominant bus level is actively driven by the transmitter and therefore stable.

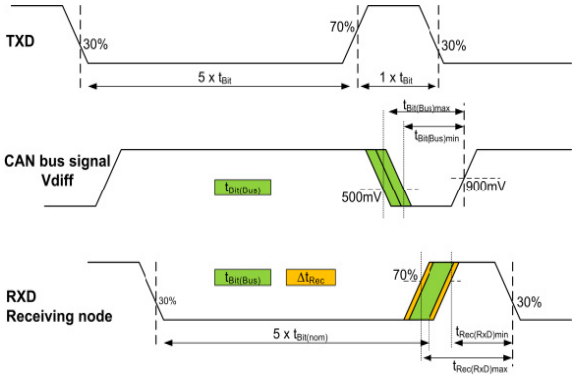

Figure 7: Recessive bit variation on a receiving node

The range marked in green is the variation of the transmitter and the range marked in yellow is the variation of the receiver. To analyze the worst case scenario, both parameters must be added. The calculation formula for $t_{Rec(RxD)}$ is:

$t_{Rec(RxD)max} = t_{Bit(Bus)max} + \Delta t_{Recmax}$

$t_{Rec(RxD)min} = t_{Bit(Bus)min} + \Delta t_{Recmin}$

Table 4: Recessive bit time at the receiving node's RxD pin

Bit rate (data-phase)	$t_{Rec(RXD)}$ (min)	$t_{Rec(RXD)}$ (max)	t_{bit} (nominal)	Load on RxD
1 Mbit/s	n.a.	n.a.	1000 ns	15 pF
2 Mbit/s	370 ns	570 ns	500 ns	15 pF
5 Mbit/s	110 ns	225 ns	200 ns	15 pF

Table 4 shows the min and max values for the recessive bit length seen by a receiving node. Please take into account that the following effects are not considered, the behaviour of the network itself, like ringing or additional propagation delay of the dominant to recessive transition, and clock tolerances.

Symmetry for networks up to 2 Mbit/s

For bit rates between 1 Mbit/s and 2 Mbit/s a transceiver specified for 2 Mbit/s should be chosen. This chapter shows the possibility to calculate the jitter at the RxD pin at the receiving node, for bit rates below 2 Mbit/s. The maximum and minimum recessive bit length $t_{Rec(RxD)}$ seen be the receiving node is calculated.

$t_{Rec(RxD)max} =$

$t_{nom} + (t_{Bit(Bus)max} - t_{nom(2Mbit/s)}) + \Delta t_{Recmax}$

$t_{Rec(RxD)min} =$

$t_{nom} + (t_{Bit(Bus)min} - t_{nom(2Mbit/s)}) + \Delta t_{Recmin}$

A calculation example for 1Mbit/s:

- loop delay symmetry deviation for 2Mbit/s transceiver (see Table 1)
  min: -100ns = (400ns - 500ns)
  max: +50ns = (550ns - 500ns)

  => $t_{Bit(RxD)}$ range @ 1Mbit/s:
  900ns (1000ns - 100ns) ≤ $t_{Bit(RxD)}$ ≤ 1050ns (1000ns +50ns)

- Transceiver Tx delay symmetry deviation for 2Mbit/s transceiver (see Table 2)
  min: -65ns = (435ns - 500ns)
  max: +30ns = (530ns - 500ns)

  ➔ $t_{Bit(Bus)}$ range @ 1Mbit/s: 935ns (1000ns – 65ns) ≤ $t_{Bit(RxD)}$ ≤ 1030ns (1000ns +30ns)

- Transceiver Rx delay symmetry deviation for 2Mbit/s transceiver
  min: -65ns
  max: +40ns

The received recessive bit time $t_{Rec(RxD}$ range for the receiving node @ 1 Mbit/s:
$t_{Rec(RxD)min}$:
870ns (1000ns + (- 65ns) + (- 65ns))
$t_{Rec(RxD)max}$:
1070ns (1000ns + 30ns + 40ns).

Symmetry for networks up to 5 Mbit/s

For bit rates up to 5Mbit/s a transceiver specified for 5Mbit/s should be chosen. This chapter shows the possibility to calculate the jitter at the RxD pin at the receiving node, for bit rates below 5 Mbit/s. The maximum and minimum recessive bit length $t_{Rec(RxD)}$ seen be the receiving node is calculated.

Maximum $t_{Rec(RxD)}$ = nominal bit time + max TX delay sym. deviation + max value of $\Delta t_{Rec\ for\ 5Mbit/s}$

Minimum $t_{Rec(RxD)}$ = nominal bit time + min TX delay sym. deviation + min value of $\Delta t_{Rec\ for\ 5Mbit/s}$

Maximum recessive bit time $t_{Rec(RxD)}$) = nominal bit time +(210ns – 200ns) + max value of $\Delta t_{Rec\ for\ 5Mbit/s}$

Minimum recessive bit time $t_{Rec(RxD)}$) = nominal bit time -(200ns – 150ns) - min value of $\Delta t_{Rec\ for\ 5Mbit/s}$

A calculation example for 4 Mbit/s:

- loop delay symmetry deviation for 5 Mbit/s transceiver (see Table 1)
  min: -80ns = (120ns - 200ns)
  max: +20ns = (220ns - 200ns)

=> $t_{Bit(RxD)}$ range @ 4Mbit/s: 170ns (250ns - 80ns) ≤ $t_{Bit(RxD)}$ ≤270ns (250ns +20ns)

- Transceiver Tx delay symmetry deviation for 5Mbit/s transceiver (see Table 2)
  min: -45ns = (155ns - 200ns)
  max: +10ns = (210ns - 200ns)

=> tBit(Bus) range @ 4Mbit/s: 200ns (250ns – 50ns) ≤ tBit(RxD) ≤ 260ns (250ns +10ns)

Transceiver Rx delay symmetry deviation for 5 Mbit/s transceiver.
min: -45ns
max: +15ns

The received recessive bit time $t_{Rec(RxD)}$ range for the receiving node @ 4Mbit/s:
$t_{Rec(RxD)min}$:
155ns (250ns + (- 50ns) + (- 45ns))

$t_{Rec(RxD)max}$:
275ns (250ns + 10ns + 15ns).

These values consider only the influence of the Transceiver. Additional effects like clock tolerance and the phase shift of the network will be discussed in the CiA 601 part 3.

The new ISO 11898-2

The current ISO 11898-2 version is meanwhile 12 years old and two additional specifications were developed to cover remote wake up features (ISO 11898-5) and partial network function (ISO11898-6). In the new ISO 11898-2 this three specifications are merged into one. New parameters are added to specify higher bit rates for CAN FD applications and existing parameter

were adjusted to prepare the specification for future needs. In the following chapter the parameters will be described in detail.

Receiver state differential voltage range

Compared to the existing specification, the differential voltage range for recessive and dominant state is extended from. In the old specification the range was specified from -1V to 5V. In real application, the voltage range is higher than expected and during bus short to ground, to supply voltage or if a ground shift is present, the differential voltage can be higher than 5V. Also a higher ground shift up to 3V is taken into account. The new range is specified from -3V to +8V. The common mode range is also added as condition. The parameters are listed in

Table 5: Differential input voltage range

Parameter	Sym	Min	Max	Unit	Condition
Recessive state differential input voltage range bus biasing active	V_{diff}	-3	+0,5	V	-12 V ≤ V_{CAN_H} ≤ +12 V -12 V ≤ V_{CAN_L} ≤ +12 V
Recessive state differential input voltage range bus biasing active	V_{diff}	+0,9	+8	V	-12 V ≤ V_{CAN_H} ≤ +12 V -12 V ≤ V_{CAN_L} ≤ +12 V
Recessive state differential input voltage range bus biasing inactive	V_{diff}	-3	+0,4	V	-12 V ≤ V_{CAN_H} ≤ +12 V -12 V ≤ V_{CAN_L} ≤ +12 V
Dominant state differential input voltage range bus biasing inactive	V_{diff}	+1,15	+8	V	-12 V ≤ V_{CAN_H} ≤ +12 V -12 V ≤ V_{CAN_L} ≤ +12 V

Internal resistance

The min value of the internal resistances is changed 5 kΩ to 6kΩ and 10 kΩ to 12 kΩ to allow a higher number of nodes in a network.

Table 6: Differential input resistance

Parameter	Sym	Min	Max	Unit	Condition
Differential internal resistance	R_{diff}	12	100	kΩ	
Single internal resistance	R_{CAN_H} R_{CAN_L}	6	50	kΩ	

Maximum ratings

In the ISO 11898-5/-6 the max ratings were increased dramatically and linked to automotive supply voltage classes. In the updated version, the maximum ratings are now independent from automotive supply voltages. A new parameter is added to limit the maximum voltage difference between the both bus pins.

Table 7: Maximum ratings

Parameter	Sym	Min	Max	Unit	Condition
General maximum ratings	V_{CAN_H} V_{CAN_L}	12	100	V	
Extended maximum rating on CAN_H, CAN_L	V_{CAN_H} V_{CAN_L}	6	50	V	Option
Maximum rating for V_{diff}= (V_{CAN_H}- V_{CAN_H})	V_{DIFF}	-5	+10	V	

Leakage currents on bus pins

The leakage currents of the bus pins are reduced to 10μA in unpowered state. This guarantees a reliable communication with low emission if one or more ECU's in a network are unsupplied due to corrupted supply line partial supplied networks.

Table 8: Transceiver Rx delay symmetry characteristics

	Sym	Min	Max	Unit	Condition
Leakage current on CAN_H, CAN_L all supplies connected to ground	I_{CAN_H} I_{CAN_L}	-10	+10	V	V_{CAN_H}= 5V; V_{CAN_L}= 5V;

Max current on CAN_H, CAN_L

To protect external components like
- Common mode choke
- Termination resistors

against overload during bus short to ground or short to supply, the output current of the transmitter output stages are limited. The voltage range for short circuit currents on CAN_H, CAN_L covers the supply voltage range of automotive 12V board net application and the min value (-3V) include ground shift of the transmitting node.

Table 9: Maximum driver output current

Parameter	Sym	Min	Max	Unit	Condition
Absolute current CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}		115	mA	-3 V ≤ V_{CAN_H} ≤ +18 V -3 V ≤ V_{CAN_L} ≤ +18 V

Transmit dominant time out

In case of a permanent dominant signal on TxD, the bus will be blocked as long as the TxD signal is dominant. To release the bus in such kind of failure cases,

the transmitter has a dominant time out feature implemented. This implementation switches off the CAN_H CAN_L output driver after the defined transmit dominant time out. Two different timings are specified. The tdom_short with a minimum of 300 µs allows a min bit rate of 50 kBit/s (calculated with 17 dominant bits in a row in an error frame) and the tdom_long for 20 kBit/s. The max value defines the min possible latency time of a system.

Table 10: Transmit dominant timeout

Parameter	Sym	Min	Max	Unit	Condition
Transmit dominant time out long	t_{dom_long}	0,8	10	ms	
Transmit dominant time out short	t_{dom_short}	0,3	5	ms	Option

Dominant output voltage characteristic

In some network concepts, all nodes are terminated to reduce the reflection on the network. Two nodes are terminated with 120 Ω and all other nodes with a higher resistance like 6 kΩ or 8 kΩ. This concept reduces the possible number of nodes in a network. To make a higher number of nodes possible the min bus load is extended from 50 Ω to 45 Ω. In future CAN networks, the diameter becomes smaller and smaller and the resistivity of the wire becomes more importance. In Figure 8 a possible scenario is demonstrated. The load resistance for Node 3 is 70 Ω.

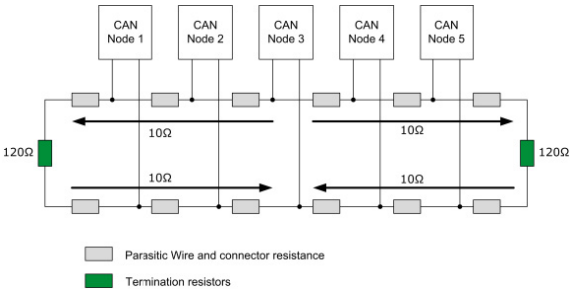

Figure 8: bus load for node 3

In the new ISO the differential for extended bus load range is limited. Also a very specific test is added and called Differential voltage in effective resistance during arbitration (and acknowledge). During acknowledge all nodes transmit a dominant signal except the transmitting node itself. If these transmitters are supplied from a high voltage level like 12 V the voltage level on the bus may become very high levels. This ends in a very long dominant signal because the bus will be only discharged by the resistive bus network. To limit this extension, the max allowed voltage level is specified.

Table 11: Transceiver dominant output characteristics

Parameter	Sym	Min	Max	Unit	Condition
Differential voltage on effective resistance during arbitration	V_{diff}	1,5	5	V	RL≤ 2240Ω
Differential voltage on extended bus load range	V_{diff}	1,4	3,3	V	45 Ω ≤ RL ≤ 70 Ω

WUP (Wake up pattern) detection

In case of bus silence, all supplied nodes are in low power mode and the current consumption in all nodes is reduced to a minimum. The transceivers are monitoring the bus with a low current consumption receiver. To avoid unwanted wake up events due to spices and noise on the bus, the wake up mechanism is new defined.
In low power mode the transceiver is in state INI (see Figure 9) and the bus biasing is off (internal resistors are connected to ground). The low power receiver in the transceiver is monitoring the bus to detect a dominant level longer than tfilter (see Table 12) on the bus. If such an event is detected the transceiver changes to state 1 and is monitoring the bus to detect a recessive level longer than tfilter (see Table 12). If the recessive condition is fulfilled the transceiver change to state 2 and starts the detection of a dominant condition again.

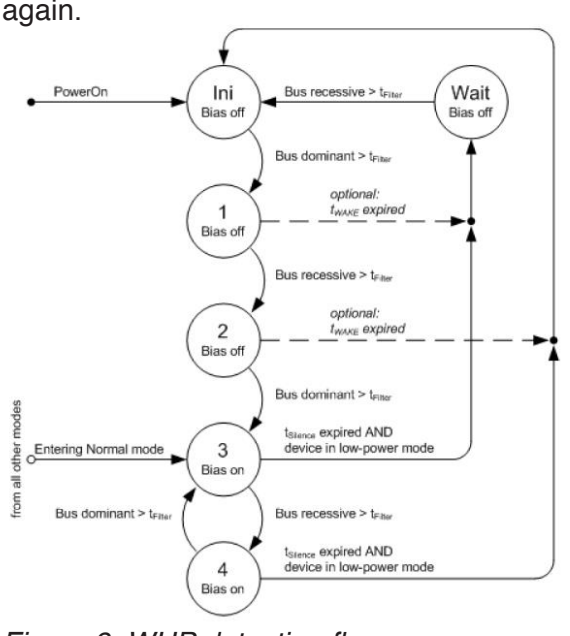

Figure 9: WUP detection flow

If the dominant condition is detected a second time the transceiver changes to state 3. The transceiver is now woken up, the bus biasing is switched on, and the wake event will be flagged on the RxD pin. In case of a permanent dominant level on the bus for example caused by a short to supply, the transceiver enters state 1 and the twake timer is started. After twake timer is expired the transceiver changes into the state WAIT. A recessive level on the bus drives the transceiver into mode INI and the transceiver can be woken up with the next CAN frame.

Table 12: CAN activity filter time

Parameter	Sym	Min	Max	Unit	Condition
CAN activity filter time, long	t_{filter}	0,5	5	µs	1,2V ≤ V_{diff} ≤ 3V -10,8V ≤ V_{CAN_H} ≤ 12,0V -12,0V ≤ V_{CAN_L} ≤ 10,8V
CAN activity filter time, short	t_{filter}	0,15	1,8	µs	1,2V ≤ V_{diff} ≤ 3V -10,8V ≤ V_{CAN_H} ≤ 12,0V -12,0V ≤ V_{CAN_L} ≤ 10,8V

The condition tfilter can be fulfilled if three dominant bits in a row are part of the ID. To improve the reliability of the WUP mechanism a short filter time is defined. Two different parameters (short and long) are specified to cover different bit rates and latency timings. (see Table 13)

Table 13: CAN activity wake up time

Parameter	Sym	Min	Max	Unit	Condition
Wake up time, long	t_{filter}	800	100000	µs	
Wake up time, short	t_{filter}	350	100000	µs	

Bus bias reaction time

The bus biasing time is the reaction time of the bus biasing after a detected WUP. The test condition is now defined. The test for the timing starts with the first dominant level condition on the bus and stops with if 10% of the bus biasing voltage level is achieved. The new test condition is illustrated in Figure 10. The modified parameter is shown in Table 14.

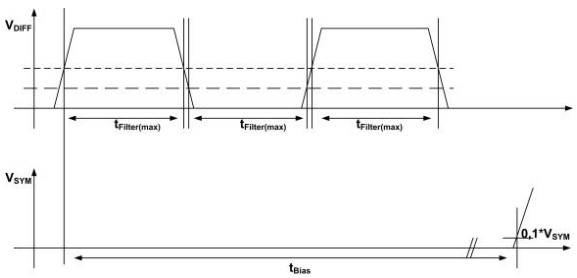

Figure 10: Bus bias reaction time definition

Table 14: Bus biasing reaction time

Parameter	Sym	Min	Max	Unit	Condition
Bus biasing reaction time	t_{bias}		250	µs	

Partial network transceiver

The partial network specification ISO 11898-6 is now part of the ISO11898-2. No parameters are changed but some descriptions are improved. For CAN FD application a new feature is added. Normally, for Partial network transceiver CAN FD frames will be detected as erroneous frames and will increase the error counter. After 32 frames the partial network transceiver will cause a wake up. For CAN FD networks this behavior had to be improved. FBFF and FEFF frames will not lead to an increase of the transceiver internal. After receiving the recessive FDF bit followed by a dominant res bit, the decoder unit stops decoding the CAN FD frame and waits for at least 6 and at most 10 recessive bits before considering a further dominant bit as a start of frame. The next frame will be decoded correctly. During the dominant res bit after a recessive FDF bit and the SOF bit dominant levels on the bus longer than a defined time (see xxx) will be detected as a dominant signal and below the specification, this will be ignored.

Table 15: CAN FD tolerant parameter

Parameter	Sym	Min	Max	Unit
Dominant signals not considered as dominant	t_{bias}		5	%arbitration bit time; ratio 4; up to 2Mbit/s
Dominant signals not considered as dominant	t_{bias}	0,175		%arbitration bit time; ratio 4; up to 2Mbit/s
Dominant signals considered as dominant	t_{bias}		5	%arbitration bit time; ratio 10; up to 5Mbit/s
Dominant signals considered as dominant	t_{bias}	0,0875		%arbitration bit time; ratio 10; up to 5Mbit/s
SOF detection after recessive bits		6	10	Bits of arbitration bit rate 500kBit/s

Summary

With the merger of all physical layer specifications into one document the parameter for all kind of CAN transceivers are now aligned. The new parameters support the higher bit rates for CAN FD and the adjustments of the existing parameter prepares the ISO 11898-2 for the future. The new ISO 11898-2 supports now:

- a bit rates up to 5Mbit/s,
- new termination concepts
- thinner or longer wires
- more worst case scenarios
- CAN FD
- CAN Partial Network and
- CAN FD tolerance

CAN is more than 30 years old and prepared for a very long lifetime.

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