Managing the transition to robust CAN FD

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With CAN FD a reality in the automotive domain, with a key focus on bandwidth and the new ISO11898-2:2016 now published, making a robust CAN FD network still remains a challenge. This paper explains NXP's experiences in working with automotive OEMs and insights gained in network simulation.

Overview

Making a reliable CAN FD network is becoming more problematic than originally promised as a number of new effects in are becoming better understood, as bit rates are pushed higher. Ringing remains the vital challenge, primarily when transitioning from a dominant to recessive bit. This has already been discussed previously [1], as well as techniques to suppress ringing [2].

In additional to updating its transceivers to meet the new ISO11898-2:2016 specification, NXP is active in providing network simulation support to validate CAN FD networks. Insights gained are used and re-applied into our transceivers. Presented here are two key findings learnt from our interactions with our partners: the first, a simulation measurement method to ensure ringing is fully controlled in networks; the second, a new artifact that may occur in so-called "ringing optimized" networks which still has a negative effect on the network reliability.

The "corrected" sample point

Fundamentally, as arbitration remains unchanged, the critical factor to ensure robust CAN FD operation is the correct sampling of the bits in the fast phase. Here, ringing is by far the dominant factor to be managed. Due to the reduced bit time, ringing effects need to dissipate within a tighter time window and the bus signal must be stable prior to the sampling point.

The new ISO11898-2:2016 also covers new parameters related to bit time symmetry to ensure that timings of dominant bits and recessive bits are remaining controlled with the delays of the physical layer. Excessive lengthening or shortening can cause incorrect sampling, generating bit errors.

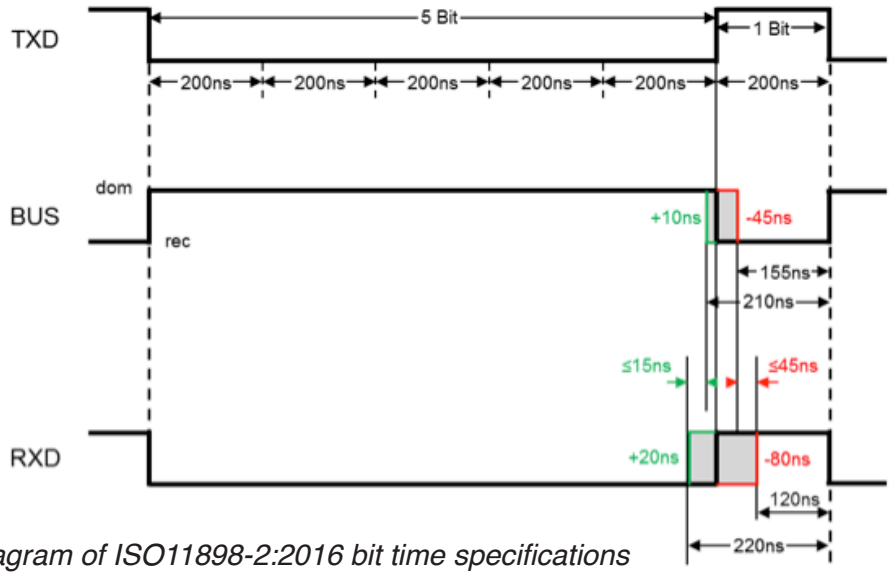

Figure 1: Diagram of ISO11898-2:2016 bit time specifications

However, due to various tolerances, there are several factors to account for, when calculating the correct point by which a node can sample and thus by when the signal shall be stable from ringing. This includes the asymmetry of the transmitter and receiver, the asymmetry of the microcontroller (MCU) interface and oscillator tolerance. These factors are summed and factored together with the nominal sample point to determine the “Corrected” Sample Point. The amount of required “correction” depends on the capabilities of the used CAN transceiver besides some other parameter.

To calculate this correction, the worst case for this effect is taken, based on 5 consecutive dominant bits (max allowed) followed by a single bit with recessive state. This takes into account the worst case oscillator tolerances across the 5 consecutive dominant bits, followed by a dominant to recessive transition. Within Figure 1, the transceiver symmetry parameters, based on a transceiver capable to drive 5Mbps, are illustrated while intentionally ignoring the propagation times through the transceiver. It purely focusses on the relative timing between the edges for easier understanding.
For a worst case topology investigation, the sending nodes MAX asymmetry has to be combined with the receiving node MAX asymmetry. This is because a transceiver may make use of the full transmitter asymmetry and compensate with its own receiver to meet the overall limit, while another receiving node may have a better transmitter but makes use of the full receiver asymmetry.

Assuming a simulation with a perfectly symmetrical transceiver model, all theoretical asymmetries of a worst case transceiver needs to be anticipated for signal assessments.

If the differential bus signal is assessed in a simulation, any included transmitter asymmetry inside of the model needs to be subtracted again, since this is already considered and avoids a double count.

Both the recessive bit and dominant bit sampling need to be corrected to be sure that this worst case is fully captured.

Recessive bit sampling at the receiving node

When calculating the recessive bit, this means:

- A transmitter asymmetry, shortening the recessive bit of up to 45 ns,
- A receiver asymmetry, shortening the recessive bit up to 45 ns,
- The sum of both is not allow to be longer than 80ns for a single transceiver device reading back its own signals.
- The worst case transceiver threshold is 0,5 V as per the ISO11898-2:2016 specification, and without any hysteresis specified, this maybe the transition point.

To check communication is robust, we calculate the Corrected Sample Point by which any signal is stable below the 0,5 V limit. This is calculated as:

Time of Nominal Sample Point (assumed as 70% of bit time), **minus**
$((2 \times t_{OSC\_Tol} \times 5,7) + t_{\mu C\_Tol} + t_{TX\_Asym} + t_{RX\_Asym})$, where:

- The Nominal Sample Point = 500 ns * 70 % = 350 ns,
- $(2 \times t_{OSC\_Tol} \times 5,7)$ is the timing deviation from two nodes with max opposite deviating oscillators of 0,3 % accuracy, over 5 bit times + the 70 % of the 6th bit time = (2 x 0,3 % x 5,7) = 17.1 ns,
- $t_{\mu C\_Tol}$ is the asymmetry of the microcontroller interface, assumed as 5 ns,
- t_{TX_Asym} is the datasheet parameter of the transmitter asymmetry (*TXD to BUS*) = 45 ns @ 5 Mbps. This is also valid for 2 Mbps as well, as this is a measure of the transceiver performance and independent of the actual bit rate.
- t_{RX_Asym} is the datasheet parameter of the receiver asymmetry (*Bus to RXD*) = 45 ns.

This equals:
350 ns minus (17,1 + 5 + 45 + 45) = 112.1 ns, for a perfect transmitter model,
350 ns minus (17,1 + 5 + 45) = 67,1 ns, for a transmitter model with transmitter asymmetry included.

Alternatively, this can be stated as ringing must be stable after 237,9 ns – or at 47,6 % of the bit time.

Dominant bit sampling at the receiving node

When calculating the dominant bit, this means:

- A transmitter asymmetry, lengthening the recessive bit of up to 10 ns,
- A receiver asymmetry, lengthening the recessive bit up to 15 ns,
- The sum of both cannot be bigger than 20 ns for a single transceiver device reading back its own signals.
- The worst case transceiver threshold is 0,9 V as per the ISO11898-2:2016 specification, and without any hysteresis specified, this maybe the transition point.

To check communication is robust, we calculate the Corrected Sample Point by which the dominant signal must remain above the 0,9 V limit. This is calculated as: *Time of Nominal Sample Point* (assumed as 70% of bit time), plus

$((2 \times t_{OSC\_Tol} \times 4,7) + t_{\mu C\_Tol} + t_{TX\_Asym} + t_{RX\_Asym} + t_Q)$, where:

- The Nominal Sample Point = 500 ns * 70 % = 350 ns,
- $(2 \times t_{OSC\_Tol} \times 4,7)$ is the timing deviation from two nodes with max opposite deviating oscillators of 0,3 % accuracy, over 4 bit times + the 70 % of the 5th bit time = (2 x 0,3 % x 4,7) = 14,1 ns,
- $t_{\mu C\_Tol}$ is the asymmetry of the microcontroller interface, assumed as 5 ns,
- t_{TX_Asym} is the datasheet parameter of the transmitter asymmetry (*TXD to BUS*) = 10 ns @ 5 Mbps,
- t_{RX_Asym} is the datasheet parameter of the receiver asymmetry (*Bus to RXD*) = 15 ns @ 5 Mbps.

This equals:

350 ns **plus** $(14,1 + 5 + 10 + 15 + t_Q)$ = 44,1 ns + 1 t_Q, for a perfect transmitter model,

350 ns **plus** (14,1 + 5 + 15) = 34,1 ns + 1 t_Q, for a transmitter model with transmitter asymmetry included.

Note, both these calculations excludes propagation delay, because this only shifts times of nodes relative to each other. Each node manages its own independent state of time based on what they synchronize to at RXD, so it does not change the overall result.

These calculations can now be used for forming assessment areas for use within simulations. If the differential signal is not entering the “not allowed areas”, the network can be verified as robust. The summarized assessment diagram for the “receiving node” is shown in Figure 2.

Bit sampling at the sending node

Sampling bits at the sending node follows a similar calculation for recessive and dominant bit calculations, however there are some key differences.

For recessive bit sampling, the Corrected Sample Point is calculated as follows:

Time of Nominal Sample Point (assumed as 70 % of bit time), minus

$(t_{\mu C\_Tol} + \{t_{TX\_Asym} + t_{RX\_Asym}\})$, where:

- $t_{\mu C\_Tol}$ is the asymmetry of the microcontroller interface, assumed as 5 ns,
- $\{t_{TX\_Asym} + t_{RX\_Asym}\}$ is the sum of the transmitter asymmetry and receiver asymmetry, which cannot be bigger than 80 ns for a single transceiver when reading back its own signal.

This calculates to (500 ns * 70 %) – (5 ns + 80 ns) = 265 ns, or 53 % of the bit time.

For dominant bit sampling, the Corrected Sample Point is calculated as follows:

Time of Nominal Sample Point (assumed as 70 % of bit time), **plus**

$(t_{\mu C\_Tol} + \{t_{TX\_Asym} + t_{RX\_Asym}\} + t_{CLK})$, where:

- $t_{\mu C\_Tol}$ is the asymmetry of the microcontroller interface, assumed as 5 ns,

- $\{t_{TX\_Asym} + t_{RX\_Asym}\}$ is the sum of the transmitter asymmetry and receiver asymmetry, which cannot be bigger than 20s for a single transceiver when reading back its own signal,
- t_{CLK} is the CAN clock before the prescaler defining the loop delay compensation of the sending node.

This can be summarized in the assessment diagram in Figure 3.

Limitations with ringing optimized topologies

A second point to be introduced related to robust CAN FD networks is the confirmation of an effect in linear or daisy chain topologies. These are often used to be "ringing optimized", by relying on stubs which are as short as possible, thus minimizing ringing effects.

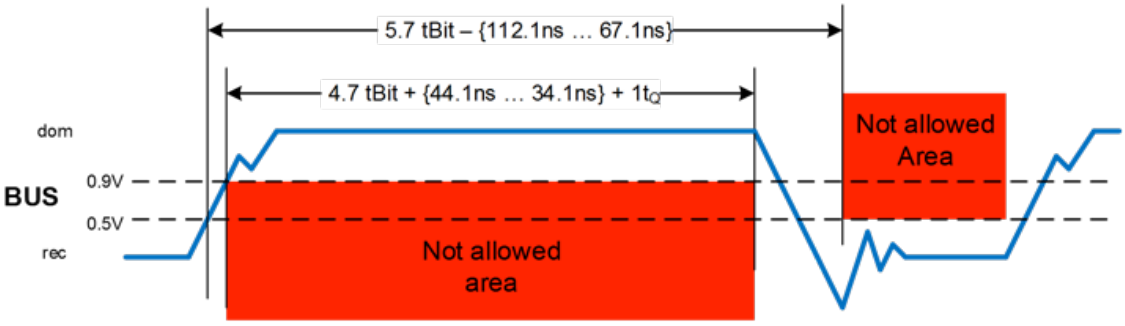

Figure 2: Assessment Diagram "Receiving Node in Network"

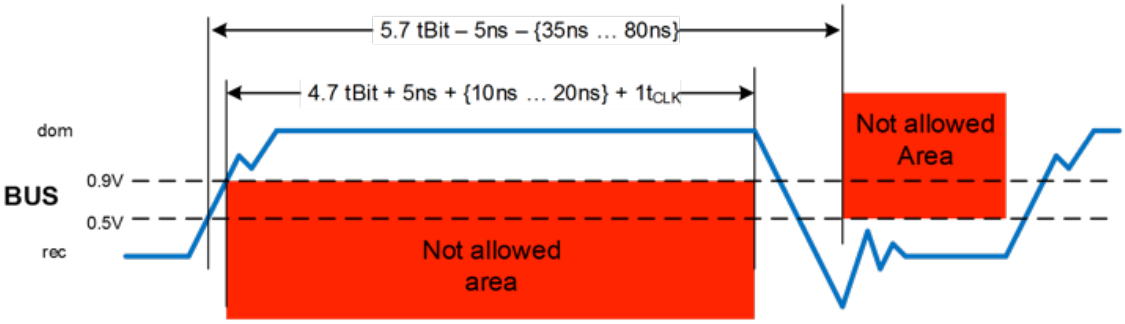

Figure 3: Assessment Diagram "Sending Node in Network"

The conclusion of this, similar to other studies [1], ensures a quantitative limit to ensure reliable networks can be guaranteed, from the perspective of the sample point. These areas marked in red can be directly applied in network simulation tools to check whether network issues are encountered. One important conclusion of this assessment is also the speed at which ringing shall be stable – as early as 47 % of the bit time for a receiving node, significantly earlier than the stated sample point.

This is not considered a preferred technique for topology design overall, as it has several drawbacks (increased cable lengths overall, non-standard connectors, less flexibility for optional nodes creating greater diversity in cabling and possibly additional complications in production line testing), but does limit the effects of ringing at higher bitrates. An example topology is shown in Figure 4. Due to the impedance of all the nodes connected in the chain, an impedance mismatch is created which forms a plateau in the differential bus signal

Figure 4: Example of a "ringing optimized" topology

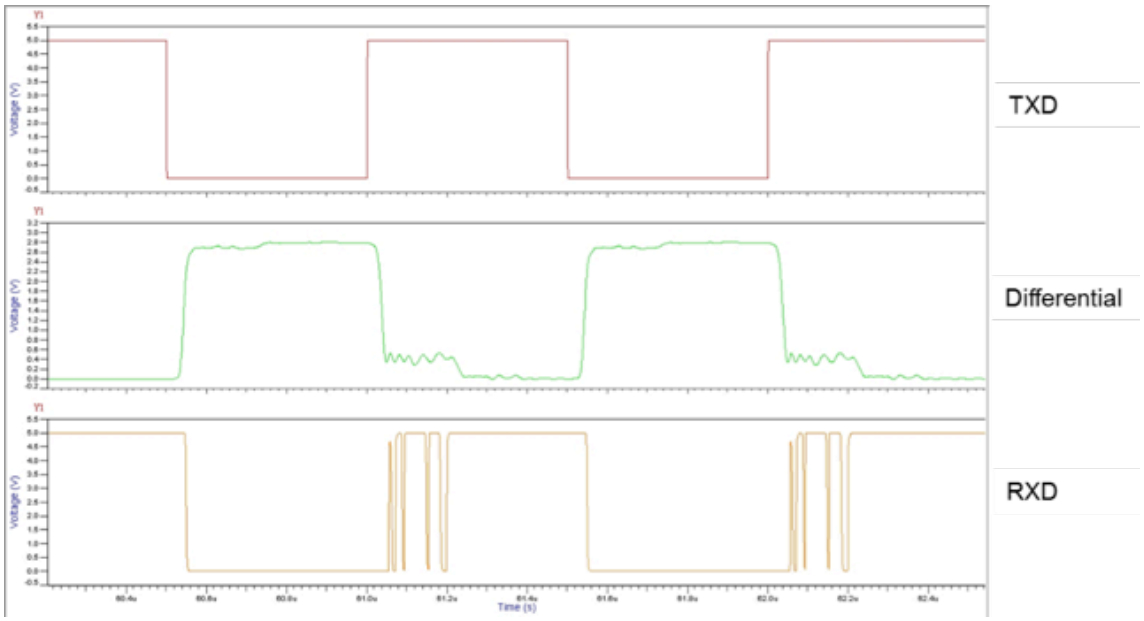

Figure 5: Effect of plateau in simulation of ringing optimized topology

at the recessive transition. In practical networks, this may form around the 0.5V receiver threshold or higher, depending on the capacitive load on the nodes. While not caused by ringing, it results in a significant portion of the bit in the fast phase not properly reaching the recessive receiver threshold and creating a potential fast jitter on the RXD signal. The more nodes are added, the more extreme this effect can become; given the analysis above, this can create a risk that the receiver threshold will not be correctly reported by the corrected or worst case sample point. Furthermore, when considering 5Mbps communication on ringing optimized topologies, this can mean that the recessive level may not be reached for the entire bit time.

Conclusion

With the ISO11898-2:2016 specification now published and parameters finalized, there are still additional items which need to be taken care of to ensure robust network operation. With proper attention, these factors can be managed to allow reliable operation, but still places limits on the overall potential for CAN FD networks. With bandwidth remaining a consistent requirement for network architectures, solutions to these challenges will need to be found to ensure CAN FD is delivering on its original potential.

References

[1] CAN FD system design – Marc Schreiner, CAN in Automation, iCC 2015, Vienna
[2] Ringing suppression technology to achieve higher data rates using CAN FD – Y. Horii, CAN in Automation, iCC2015, Vienna
[3] ISO11898-2:2016(E) – ISO, 2016-12-15

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