Characterizing the physical layer of CAN FD

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The "Classic" CAN bus has been the workhorse protocol used for automotive powertrain monitoring and control for decades. With demands for increased electronic content in next-generation automobiles, many systems are migrating to CAN FD (CAN with Flexible Data). This shift in technology to transmit and receive more bits in less time over relatively long distances brings with it new design and test challenges. This paper shows in a practical sense how to perform critical dynamic pulse parameter measurements including transceiver loop delay and recessive bit width using oscilloscopes. Also discussed is eye-diagram mask testing. Eye-diagram testing provides a physical layer analog signal quality test in one composite measurement.

Transceiver Loop Delay and Recessive Bit-width Measurements

Transceiver loop delay is defined as the time delay for bit transitions to travel from the transmit output pin (TxD) of the CAN controller, through the CAN transceiver, and then back again to the receive input pin (RxD) of the same CAN controller as shown in Figure 1[1],[2].

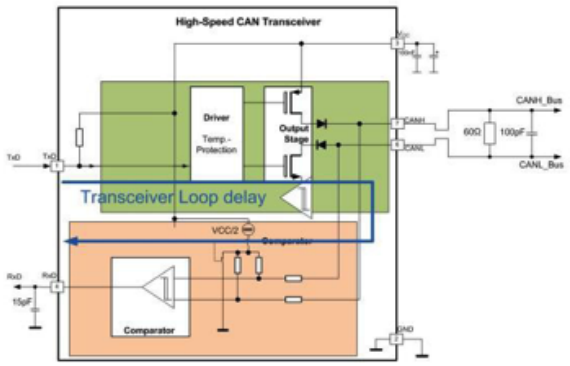

Figure 1: Transceiver loop delay[1]

Loop delay symmetry refers to the time difference for when this time delay is measured relative to dominant-to-recessive transitions ($T_{LOOP(D2R)}$) versus recessive-to-dominant transitions ($T_{LOOP(R2D)}$). Asymmetric loop delay ($T_{LOOP(D2R)} \neq T_{LOOP(R2D)}$) will contribute to shortened or lengthen bit-widths on the differential bus. As recessive bits are shortened, dominant bits are lengthened, and vice-versa. At higher CAN FD data phase bit rates, such as 8 Mbps, shortened bit-widths run the risk of either being sampled during an unstable bit transition at or near the end of the current bit-time, or possibly even sampled during the next bit-time. To insure transceiver loop delay symmetry and differential bus bit-width timing meet required specifications, these parameters should be fully characterized using an oscilloscope.

Figure 2 shows a timing diagram of the critical measurements required to characterize transceiver loop delay symmetry and differential bus bit-width. It should be noted that the differential bus trace ($V_{DIFF(L-H)}$) is shown in a dominant-bit-low format (explained later). Most timing diagrams in other documents typically show the differential bus in a dominant-bit-high format ($V_{DIFF(H-L)}$).

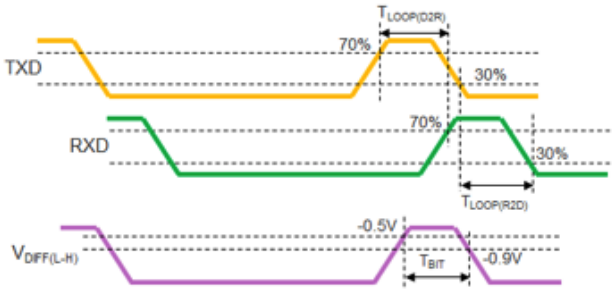

Figure 2: Transceiver loop delay and differential bit width timing diagram

The single-ended signals at TxD and RxD of the CAN controller can be probed using standard high-impedance passive probes relative to system ground. However, it is

[1] *Transceiver graphic provided by Infineon Technologies*

recommended that you use a differential active probe to capture the differential bus signal ($V_{DIFF(L-H)}$) for the bit-width (T_{BIT}) measurement, as opposed to using the scope's waveform math functions to compute the mathematical difference of the ground-referenced CAN_L and CAN_H signals. Not only does a differential probe utilize fewer channels of the scope, but it also provides higher common mode rejection, superior signal fidelity, and faster throughput.

When probing the differential bus with a differential active probe, you can connect the probe to CAN_H and CAN_L to capture and display the differential bus signal in either a dominant-bit-high or dominant-bit-low format. Intuitively, most engineers connect the positive (+) input of the differential probe to CAN_H and the negative (-) input to CAN_L. This will produce a view of the bus in a dominant-bit-high format, which is the opposite polarity of TxD and RxD, which are always dominant-bit-low. Alternatively, you can connect the positive input of the differential probe to CAN_L and the negative input of the probe to CAN_H to capture and view the bus in a dominant-bit-low format. All timing diagrams and measurements shown in this paper show the differential bus signal in a dominant-bit-low format.

When probing the differential bus in a dominant-bit-low format ($V_{DIFF(L-H)}$), the bit-width measurement should be performed from the upper -0.5 V threshold level to the lower -0.9 V threshold level. If probed to view dominant-bit-high ($V_{DIFF(H-L)}$), the bit-width measurement should be performed from the lower +0.5 V threshold level to the upper +0.9 V threshold level.

$T_{LOOP(D2R)}$ should be measured at the 70 % to 70 % threshold levels, while $T_{LOOP(R2D)}$ should be measured at the 30 % to 30 % threshold levels.

Although the default measurement threshold of most oscilloscopes is to measure delay times and pulse widths relative to 50 % threshold levels, most, if not all, of today's mid-range and higher-performance oscilloscopes from all vendors allow users to customize measurement threshold levels in either absolute (volts) or relative (%) levels.
To characterize loop-delay symmetry based on the transmitter half of a transceiver, the differential bit-width (T_{BIT}) measurement, as well as transceiver loop delay measurements ($T_{LOOP(D2R)}$ and $T_{LOOP(R2D)}$) should to be measured on "isolated" recessive bits preceded by 5 dominant bits and followed by 1 or more dominant bits. This pattern by definition is a stuff bit. But depending on the topology of your CAN FD network, timing measurements based on additional bit patterns should also be characterized including an isolated recessive bit (1 bit-time wide) preceded by a single dominant bit (1 bit-time wide), as well as 5 recessive bits preceded by a single dominant bit. You may discover that there are differences in symmetry based on the number of preceding dominant bits, as well as the number of recessive bits. This is especially true for higher bit rates due to the proximity of ringing after bit transitions that can affect subsequent transition timing. Inter-symbol interference[3] (ISI) is a commonly used term in high-speed jitter analysis for this phenomena where a yet-to-be-settled (non-steady-state) preceding bit transition can affect the timing of a following bit transition.

This paper focuses on just the case of setting up the oscilloscope to characterize timing symmetry based a bit pattern of an isolated recessive bit preceded by 5 dominant bits. Setting up the scope to synchronize on other bit patterns is analogous. Synchronizing the scope's acquisitions on specific serial bit patterns is the biggest challenge in performing these critical timing measurements.

Synchronizing Scope Acquisitions and Measurements on Isolated Recessive Bits

To perform the required measurements on an isolated recessive bit, you have three choices.

1. Capture a CAN FD frame, scroll through the data phase to visually identify the required bit sequence, then perform a single set of timing measurements. The drawback of this method is that you won't

be able to collect statistical measurement results to look for possible worst-case variations due to jitter and clock tolerance errors since the measurements will be based on a single-shot acquisition.

2. Program-in a null data set (all zero's). This will create an isolated stuffed recessive bit surrounded by a series of 5 dominant zero bits throughout the entire data phase. Then use the scope's time-qualified pulse-width trigger capability to trigger on five consecutive dominant bits.
3. To perform the required loop delay and bit-width measurements on live/random FD data traffic (no special data pattern), use a combination of time-qualified pulse-width triggering to trigger on 5 consecutive preceding dominant bits along with zone triggering[4] to qualify on 1 or more following dominant bits. This is the method that is documented in this paper.

Figure 3 shows the first step in setting up scope triggering to isolate recessive bits preceded by 5 consecutive dominant bits at a data phase bit rate of 8 Mbps. At this bit rate, the nominal bit time is 125 ns.

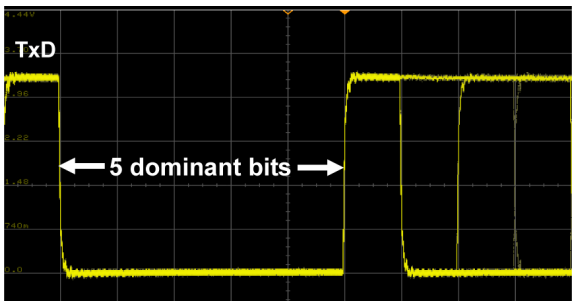

Figure 3: Triggering on 5 consecutive dominant bits.

The scope was set up to trigger on low-level pulses (dominant levels) below the trigger level threshold of TxD that occurred for > 575 ns but < 675 ns. Note that the nominal timing of 5 dominant bits would be 625 ns (5 divisions at 125 ns/div) for a CAN FD data phase based on 8 Mbps.

As shown in Figure 3, although the scope isolated five consecutive dominant bits preceding the trigger reference point (orange triangle at top of display), the overlay of waveforms from repetitive acquisitions shows recessive bits of multiple bit times following the trigger point.

Figure 4 shows the second step in isolating a single recessive bit using zone-qualified triggering. With a "must intersect" zone (yellow shaded box) placed in the timing position where recessive-to-dominant transitions should occur for a single recessive bit time (~125 ns after the pulse-width trigger point), the scope synchronized the display of acquisitions on the required isolated bit pattern.

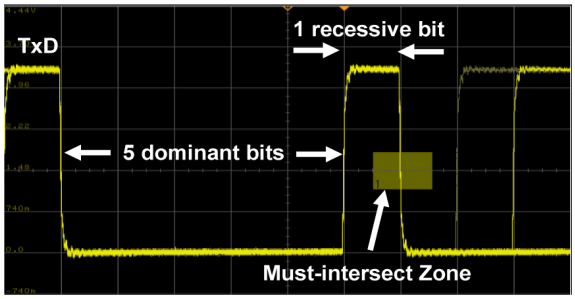

Figure 4: Isolating a single recessive bit using zone qualified triggering.

Although the scope captures recessive bits of various bit times based on just the time-qualified pulse-width trigger condition, the scope discards all captured waveforms that don't also meet the zone qualification and displays just acquisitions with recessive-to-dominant bit transitions that intersect the zone. After establishing triggering on the required isolated bit pattern of TxD, we are now ready to perform the required multi-channel transceiver loop delay and differential bus bit-width measurements.

Figure 5 shows the dominant-to-recessive loop delay measurement ($T_{LOOP(D2R)}$) from TxD (channel-1 yellow trace) at the 70 % threshold level to RxD (channel-2 green trace) at the 70 % threshold level resulting in a Δt of ~138 ns.

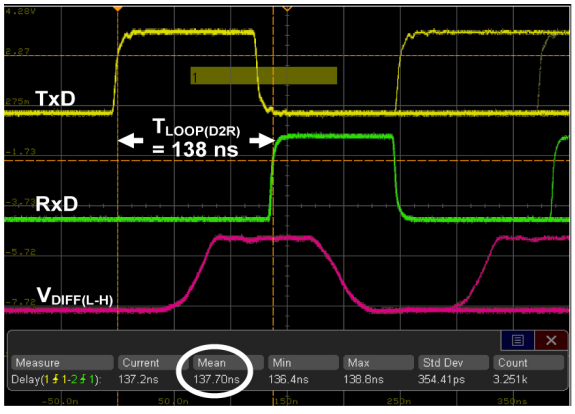

Figure 5: Dominant-to-recessive transceiver loop delay measurement.

Figure 6 shows the recessive-to-dominant loop delay measurement ($_{TLOOP(R2D)}$) from the 30 % threshold level of TxD to the 30 % level of RxD resulting in a Δt of ~122 ns.

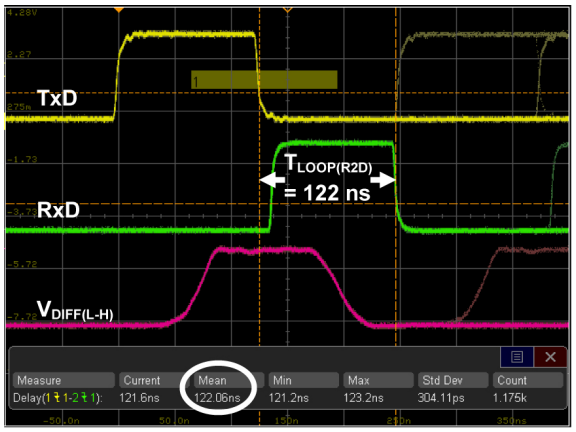

Figure 6: Recessive-to-dominant transceiver loop delay measurement.

Figure 7 shows the differential bit-width measurement (T_{BIT}) on $V_{DIFF(L-H)}$ (channel-4 red trace) from the -0.5 V threshold level to the -0.9 V threshold level.

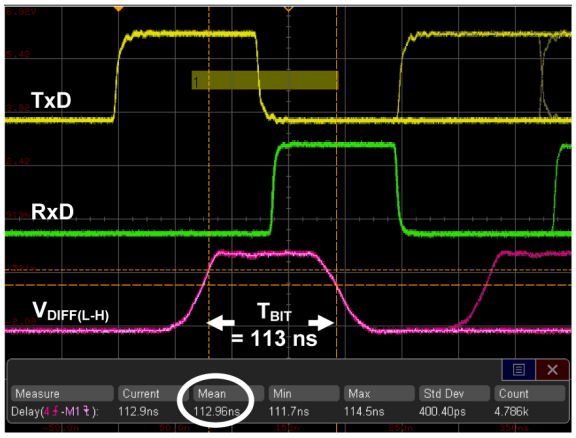

Figure 7: Differential bus bit-width measurement.

It should be no surprise that this measurement resulted in ~113 ns versus the nominal bit-width of 125 ns (12 ns difference) for an 8 Mbps FD bit rate. Asymmetric loop delay ($T_{LOOP(D2R)}$ versus $T_{LOOP(R2D)}$) resulted in a 16 ns difference. It should be noted that some of the factors that can contribute to variations in asymmetric loop delay and differential bit-width include dominant bit levels and asymmetric transition times (rising versus falling) of the differential bus.

As a side note, notice in the waveforms shown in Figures 5, 6, and 7 that the RxD recessive bit (green trace) begins after the TxD recessive bit (yellow trace) ends. Without implementation of a secondary sample point (SSP)[5], it would be impossible for this controller to monitor itself for bit errors.

Although the preceding measurement examples were based on just the bit pattern case of an isolated recessive bit preceded by 5 dominant bits, setting up the scope to trigger and isolate other bit patterns is very similar using the scope's time-qualified pulse-width triggering along with zone qualification.

Eye-diagram Mask Testing

Eye-diagram mask testing[6] is used in a broad range of today's higher-speed serial bus applications. An eye-diagram is basically an infinite-persisted overlay of all bits captured repetitively by an oscilloscope to show when bits are valid. This provides a composite picture of the overall quality of a system's physical layer characteristics which includes amplitude variations, timing uncertainties, and infrequent signal anomalies. Eye-diagram testing is especially important for higher speed buses such as the new CAN FD serial bus.

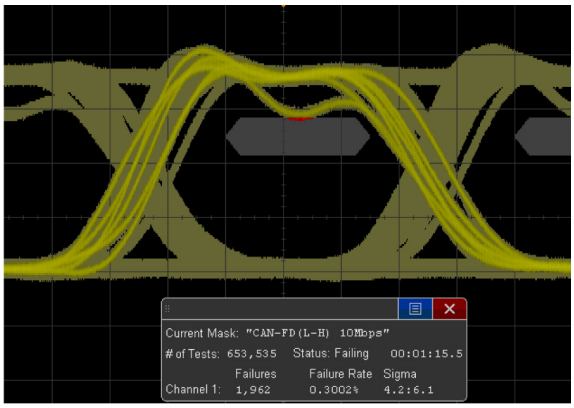

Figure 8: Eye-diagram mask test on CAN FD data phase bits.

Figure 8 shows a CAN FD eye-diagram test based on probing to view the differential bus in a dominant-bit-low format ($V_{DIFF(L-H)}$). Creating an eye-diagram requires a clock recovery algorithm to place bit transitions relative to clock resynchronization points which occur on every recessive-to-dominant bit transition. Between these resynchronization bit transitions, digitized waveforms are "sliced" into nominal bit times based on the

scope's timebase used as an ideal timing reference. Note that the timebase of today's oscilloscopes are much more accurate (typically specified within a few parts per million or less) as compared to CAN system clocks.

Oscilloscope eye-diagram displays basically show if dominant and recessive bits have settled to valid/specified levels prior to receiver sampling, which typically occurs near the 60% sample point during the FD data phase. In other words, the CAN FD eye-diagram shows what the CAN receiver "sees" by synchronizing the scope's acquisition and display timing to the CAN FD receiver's timing. The result is a single oscilloscope measurement that provides insight into the overall signal integrity of the CAN FD physical layer network to show worst-case timing and worst-case vertical amplitude variations.

On the vertical axis, the eye-diagram display shows various peak-to-peak amplitudes. Variations in signal amplitudes on the differential CAN FD bus are primarily due to the following:

- System noise/interference/coupling
- Different transmitters (nodes in the system) exhibiting unique and different output characteristics
- Attenuated amplitudes due to network lengths, reflections, and terminations

Although variations in peak-to-peak amplitudes on a limited number of bits can also be observed when viewing the bits and frames sequentially (non eye-diagram display), the eye-diagram shows these variations — along with details of pulse shapes that may reveal termination problems — in a single overlaid picture of all bits.

On the horizontal axis, the eye-diagram display shows timing uncertainties primarily due to the following:

- Worst-case clock jitter
- Worst-case clock tolerance between various nodes in the system
- Bit-time quantization (typically 1/8th to 1/25th of 1 bit-time)

Worst-case timing errors such as these are extremely difficult to observe when viewed as a sequential waveform (non eye-diagram display).

Interpreting the Pass/Fail Mask

Overlaid and infinitely persisted bits of the eye-diagram are continually compared against a 6-point polygon-shaped pass/fail mask (gray zone). Although this mask shape is typical for many of today's higher-speed serial bus standards, the ISO 11898-2 specification has not yet specified a defined shape nor boundaries for CAN FD eye-diagram mask testing.

The mask defines a failing region where signals are not supposed to enter. You can think of this region on the scope's display as the "keep-out" zone. If captured waveforms enter this zone on this scope's display, the scope will display those portions of the waveform trace in red as shown in Figure 9. In addition, the scope will count the number of bits that fail the test, the total number of bits tested, and also provides failure rate statistics.

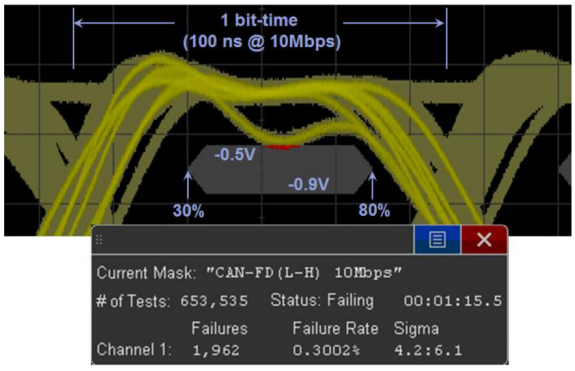

Figure 9: Comparing each dominant and recessive bit against a pass/fail mask.

The top and bottom boundaries of the mask are based on specified worst-case CAN FD receiver threshold levels of -0.5 V to -0.9 V (for dominant-bit low probing). In this particular CAN FD eye-diagram mask test, we can see that one of the system's nodes generates a recessive bit (high level) that rings and dips down into the failure zone near the top of this mask. Note that the portion of the waveform that violates the -0.5V threshold level is highlighted in red. This test reveals that there may be a risk

that this “dip” in the differential signal could be interpreted by CAN FD transceivers as a dominant bit. We can also see that this CAN FD system generates approximately 20 ns of peak-to-peak timing uncertainty over the worst-case 10 bit-times that are tested. This timing uncertainty could be due to either clock tolerance error and/or random jitter. And finally, the mask test statistics window shows us that the failure rate for this test was approximately 0.3 % based on testing more than 650,000 bits over a total test time of approximately 75 seconds.

Summary

As timing constraints of data-valid windows tighten due to increased data rates of CAN-based designs as they transition from “Classic” CAN architectures running at 500 kbps to higher-speed CAN FD architectures running at rates up to 8 Mbps during the data phase, it becomes more important to test and verify that critical dynamic pulse parameter timing, including transceiver loop delay symmetry and differential bus recessive bit width, meet required specifications to ensure that designs operate reliably under all conditions.

The primary measurement tool used today to measure and characterize these timing parameters is a 4-channel oscilloscope with two standard high-impedance passive probes and a differential active probe. As discussed in this paper, the timing measurements themselves are relatively easy to perform on most of today’s digital oscilloscopes based on user-defined measurement threshold levels. A high-performance and high-priced oscilloscope is not required. A 4-channel oscilloscope with 200 MHz bandwidth and a sample rate of 2 GSa/s or higher is more than sufficient.

The biggest challenge in performing these measurements is often just determining how best to set up the scope to perform the measurements on isolated recessive bits embedded within “live” data traffic (not a predetermined and preprogrammed bit pattern). This paper showed how to use an oscilloscope’s time-qualified pulse-width triggering in conjunction with zone-qualified triggering to isolate the scope’s acquisitions and measurements on isolated bits (recessive bit preceded by five dominants bits and followed by one or more dominant bits).

Also discussed in this paper was CAN FD eye-diagram mask testing. With the proper clock recovery algorithm, eye-diagram measurements will provide you with a composite picture of overlaid bits relative to the ideal clocking allowing you to quickly make judgements about your CAN FD system’s noise, jitter, reflections, clock tolerances, bit levels, and bit timing.

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References

[1] Maria-Magnus Hell, Infineon Technologies, The physical layer in the CAN FD world – The update, iCC 2015 proceedings
[2] Orlando Esparza, Wilhelm Leichtfried, Fernando Gonzalez, Microchip Technology Inc., Transitioning applications from CAN 2.0 to CAN FD, iCC 2015 proceedings
[3] Choosing the ISI Filter Size for EZJIT Plus Arbitrary Data Jitter Analysis, Keysight Technologies application note, page 3, publication number 5989-4974EN
[4] Johnnie Hancock, Keysight Technologies, Triggering on Infrequent Anomalies and Complex Signals using InfiniiScan Zone, Keysight application note, publication number 5991-1107EN
[5] Florian Hartwich, Robert Bosch GmbH, CAN with Flexible Data-Rate, iCC 2012 proceedings
[6] Johnnie Hancock, Keysight Technologies, CAN FD Eye-diagram Mask Testing, Keysight application note, publication number 5992-0437EN